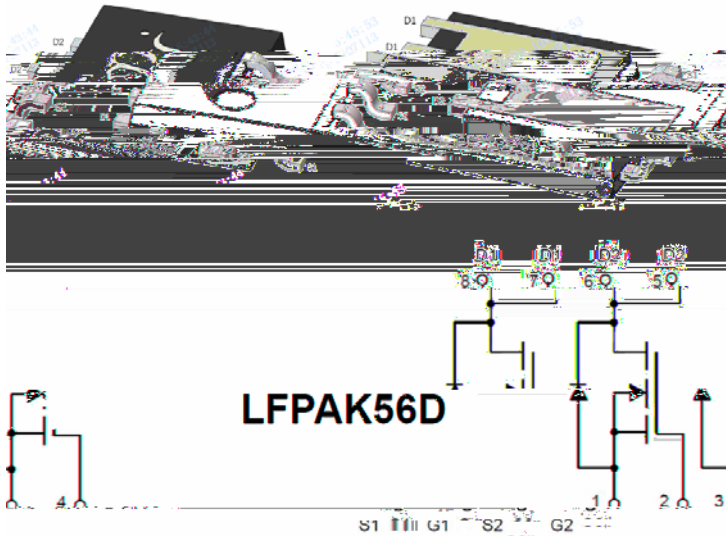




N-Channel Enhancement Mode Field Effect Transistor



Product Summary

χ V_{DS}	40V	
χ I_D	69A	
χ $R_{DS(ON)}$ (at $V_{GS}=10V$)	5.8m Ω	mbol

				Limit	Unit
Drain-source Voltage			V_{DS}	40	V
Gate-source Voltage			V_{GS}	020	V
Continuous Drain Current (Note 1,2)	Steady-State	$T_A=25^\circ\text{C}$, $V_{GS}=10\text{V}$	I_D	14	A
		$T_A=100^\circ\text{C}$, $V_{GS}=10\text{V}$		10	
Continuous Drain Current (Note 1,3)	Steady-State	$T_C=25^\circ\text{C}$, $V_{GS}=10\text{V}$		69	
		$T_C=100^\circ\text{C}$, $V_{GS}=10\text{V}$		48	
Pulsed Drain Current	$T_C=25^\circ\text{C}$, $t=100\mu\text{s}$		I_{DM}	270	A
Avalanche energy	$V_G=10\text{V}$, $R_G=25\Omega$, $L=0.5\text{mH}$, $I_{AS}=16\text{A}$		EAS	64	mJ
Total Power Dissipation (Note 1,2)	Steady-State	$T_A=25^\circ\text{C}$ 3			
			P_D		W
		$T_C=25^\circ\text{C}$		65	
		$T_C=100^\circ\text{C}$		32	
Junction and Storage Temperature Range			T_J, T_{STG}	-55 +175	

Thermal resistance

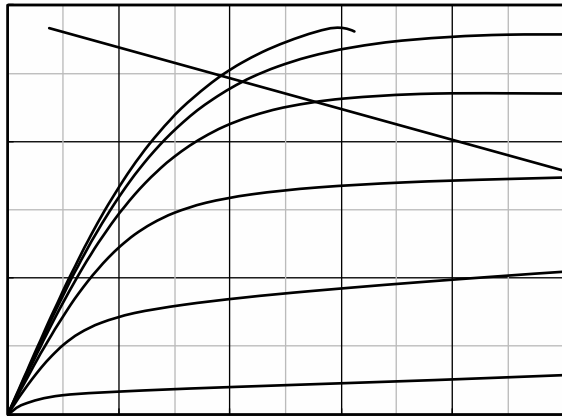
Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	R_{JA}	40	50	/W
Thermal Resistance Junction-to-Case	Steady-State	R_{JC}	1.8	2.3	

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJYAD5D8G04HRHQ	F1	YAD5D8G04HR	5000	10000	100000	13'6" reel



■ Typical Electrical and Thermal Characteristics Diagrams



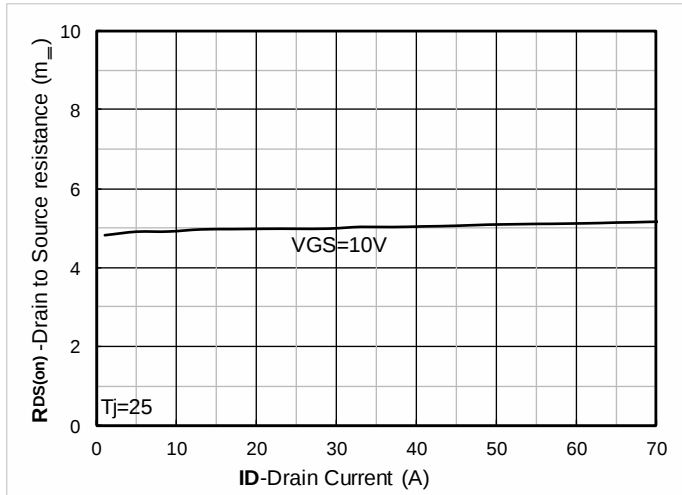


Figure 7. $R_{DS(on)}$ VS Drain Current

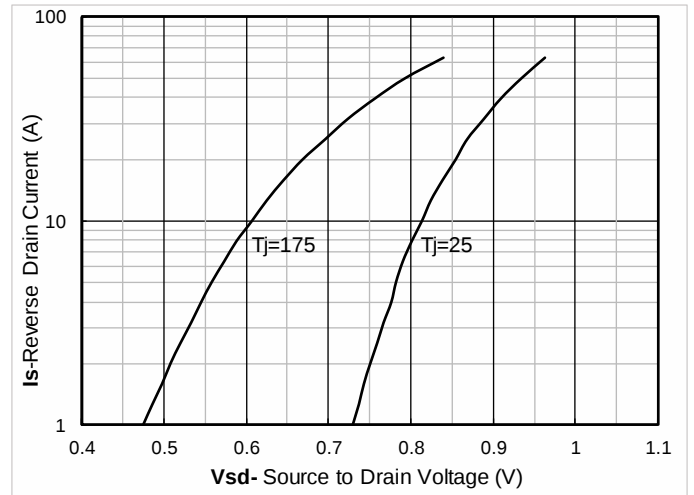


Figure 8. Forward characteristics of reverse diode

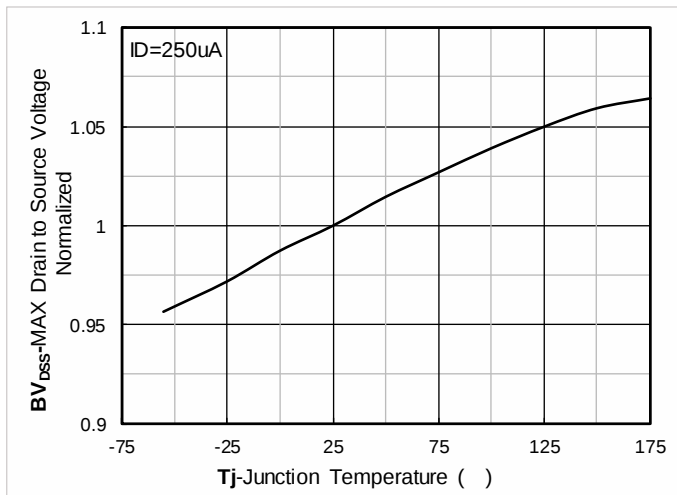


Figure 9. Normalized breakdown voltage

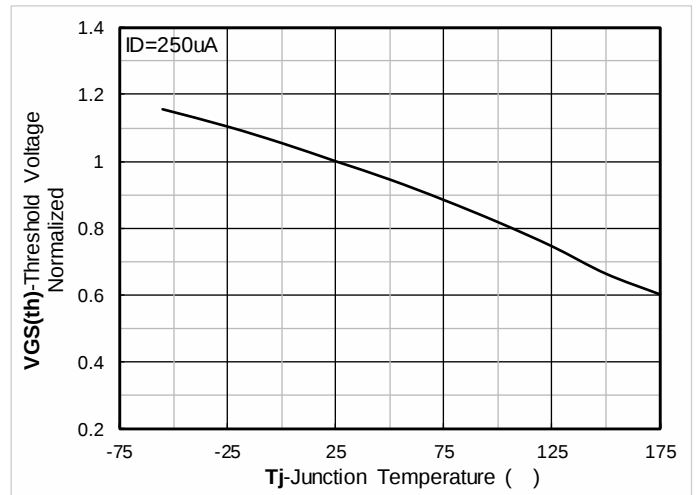


Figure 10. Normalized Threshold voltage

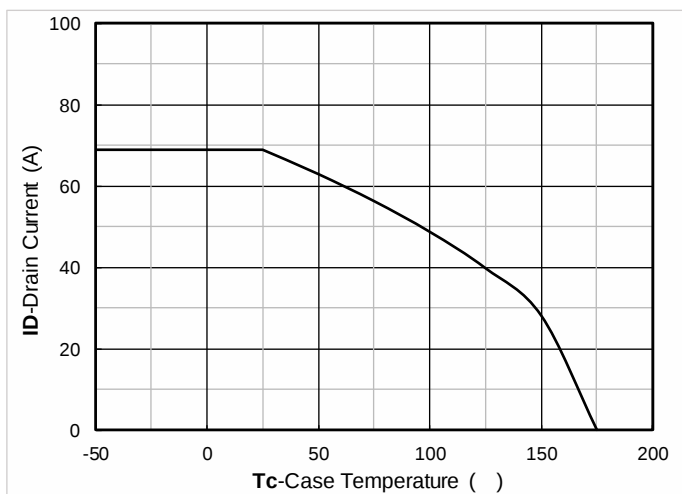


Figure 11. Current dissipation

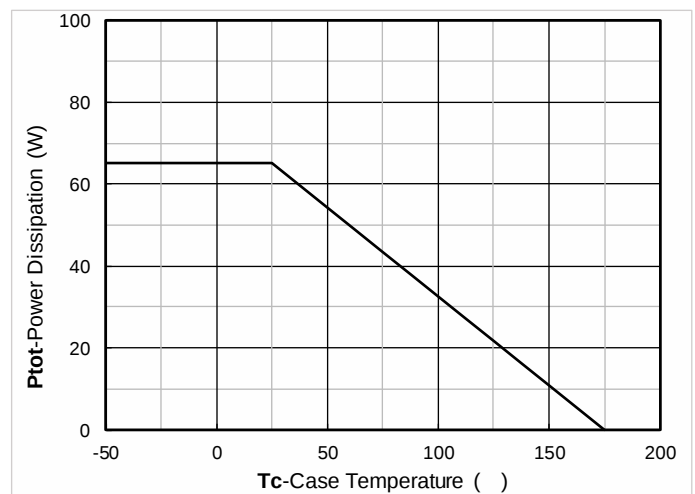
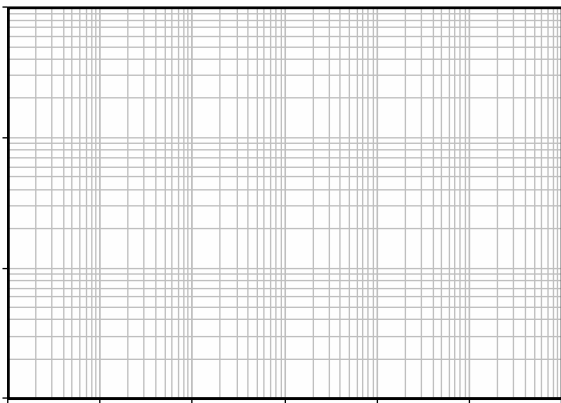


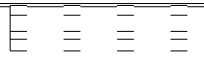
Figure 12. Power dissipation





Ω LFPAK56D Package information

1



Top View

Bottom View

Side View

Note:

- 1.Controlling dimension:in millimeters.
- 2.General tolerance:00.10mm.
- 3.The pad layout is for reference purposes only.
4. It is the key size.



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