



## N-Channel Enhancement Mode Field Effect Transistor

### Product Summary

$V_{DS}$	100 V
$I_D$	300 A
$R_{DS(ON)}$ ( at $V_{GS}=10V$ )	1.45m
$R_{DS(ON)}$ ( at $V_{GS}=6V$ )	1.9m
100% EAS Tested	
100% $V_{DS}$ Tested	

### General Description

Surface-mounted package  
Excellent package for heat dissipation  
High Density Cell Design for Low  $R_{DS(on)}$   
Moisture Sensitivity Level 1  
Epoxy Meets UL 94 V-0 Flammability Rating

### Applications

High power inverter system  
Uninterruptible power



## Typical Electrical and Thermal Characteristics Diagrams

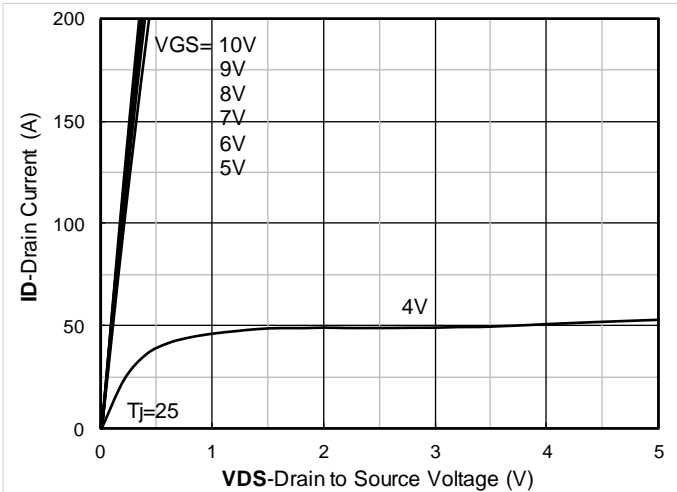


Figure 1. Output Characteristics

Figure 2. Maximum Transient Thermal Impedance

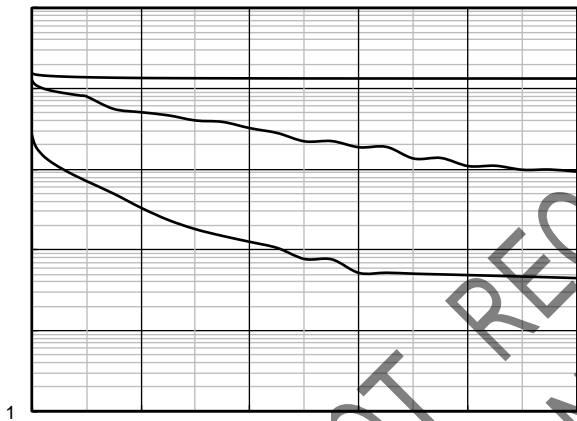


Figure 3. Capacitance Characteristics

Figure 4. Gate Charge

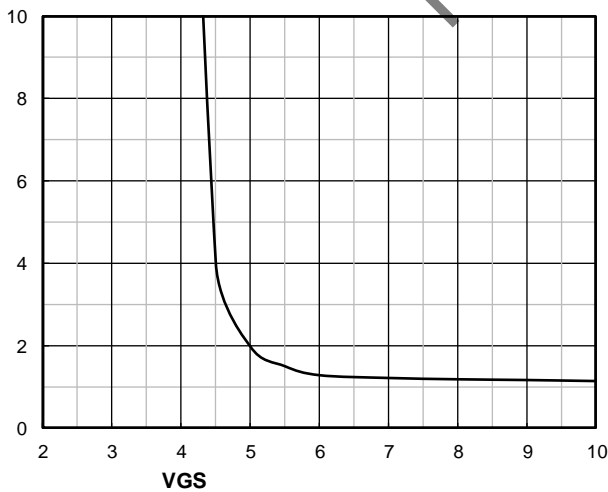


Figure 5. On-Resistance vs Gate to Source Voltage

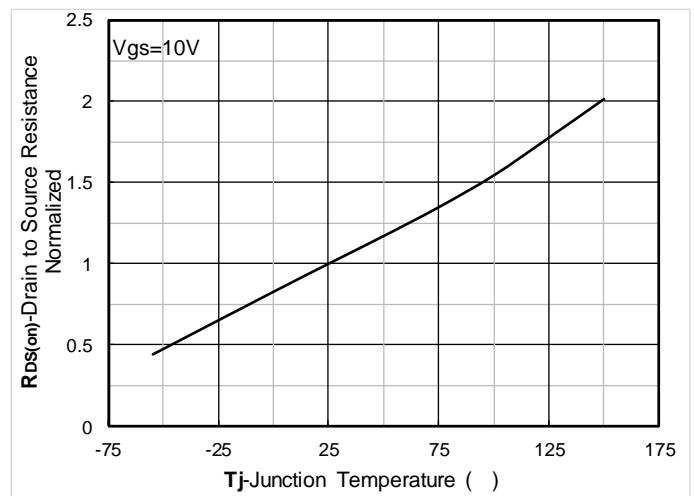


Figure 6. Normalized On-Resistance

**YJT300G10H**

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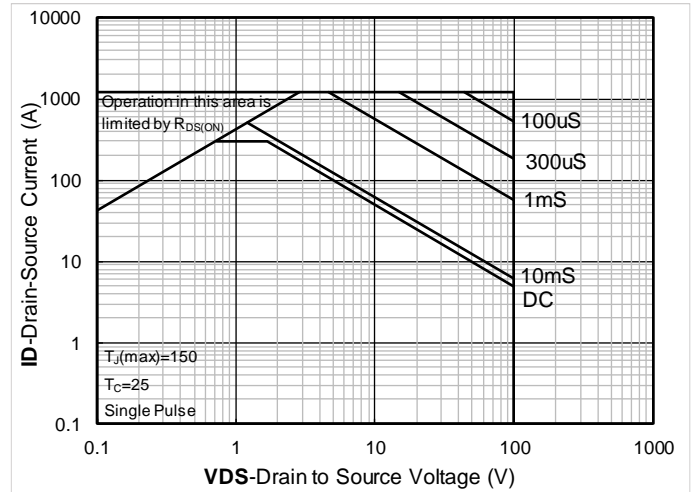
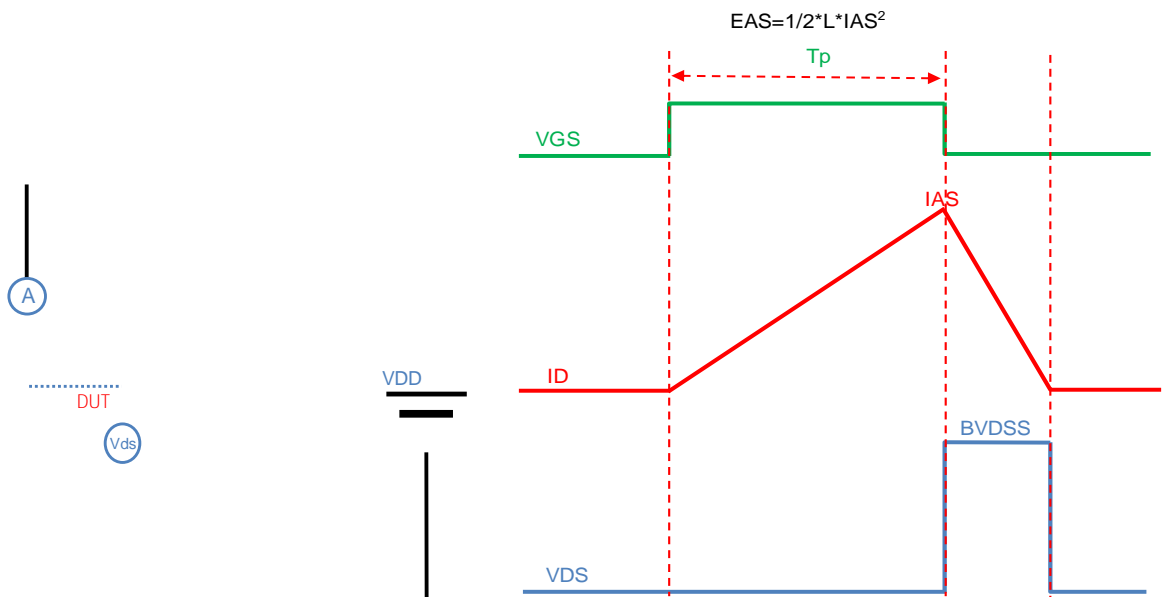


Figure 13. Maximum Transient Thermal Impedance

Figure 14. Safe Operation Area

## Test Circuits & Waveforms







## TOLL Package information

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.2	2.3	2.4
A1	1.7	1.8	1.9
b	0.7	0.8	0.9
b1	9.7	9.8	9.9
b2	1.1	1.2	1.3
c	0.4	0.5	0.6
D	10.28	10.38	10.48
D1	10.98	11.08	11.18
D2	3.2	3.3	3.4
D3	4.45	4.55	4.65
E	9.8	9.9	10
E1	8	8.1	8.2
e	1.2 BSC		
H	11.58	11.68	11.78
H1	6.95 BSC		
i	0.1 REF		
j	0.46 REF		
L	1.5	1.6	1.7
L1	0.6	0.7	0.8
L2	0.5	0.6	0.7
L3	0.3	0.4	0.5
Q	8 REF		
R	3.0	3.1	3.2

Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.03$ mm.
3. The pad layout is for reference purposes only.

NOT RECOMMENDED  
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