



P-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	-30 V
I_D	-10 A
$R_{DS(ON)}$ (at $V_{GS}=-10V$)	19 m
$R_{DS(ON)}$ (at $V_{GS}=-4.5V$)	28 m
100% EAS Tested	

General Description

Trench Power LV MOSFET technology
 High density cell design for Low $R_{DS(ON)}$
 High Speed switching
 Moisture Sensitivity Level 3
 Epoxy Meets UL 94 V-0 Flammability Rating
 Halogen Free

Applications

Battery protection
 Load switch
 Power management

Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	-30	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25$	I_D	-10	A
	$T_A=100$		-6.3	
Pulsed Drain Current ^A		I_{DM}	-80	A
Avalanche energy ^B		EAS	56	mJ
Total Power Dissipation ^C	$T_A=25$	P_D	2.5	W
	$T_A=100$		1	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 +150	

Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	Steady-State	R_{JA}	40	50	/W

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking
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Electrical Characteristics ($T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
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Static Parameter

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SOP-8 Package information

SYMBOL	MIN.		
	0.053	0.069	
B	0.004	0.010	
		0.061	
D		0.020	
E			
F			
G	0.050BSC		1.270BSC
H			
J			
K			



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