# N-Channel Enhancement Mode Field Effect Transistor

## Product Summary

- $V_{DS}$ 40V
- $I_D$ 50A
- $R_{DS(ON)}$( at $V_{GS}$=10V) 7mΩ
- 100% EAS Tested

## General Description

- Split gate [illegible]
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

## AppliQR5)]TJETQ EMC 842reW*nBT00888 0 3( s 5

## Typical Electrical and Thermal Characteristics Diagrams

Figure 1. Output Characteristics

Figure 2. Transfer Characteristics

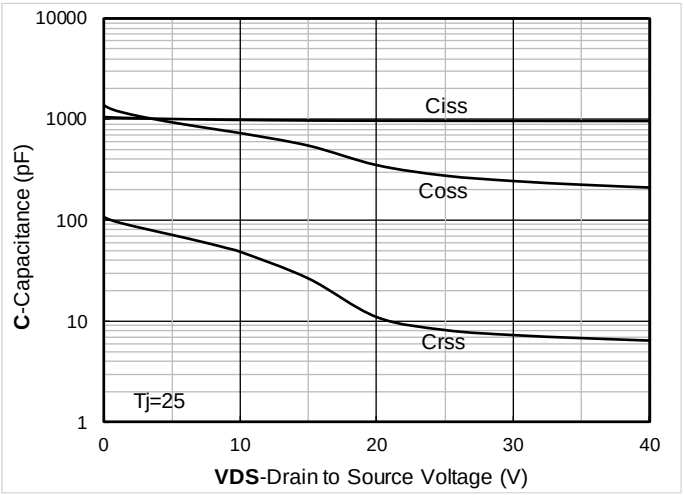



Figure 3. Capacitance Characteristics

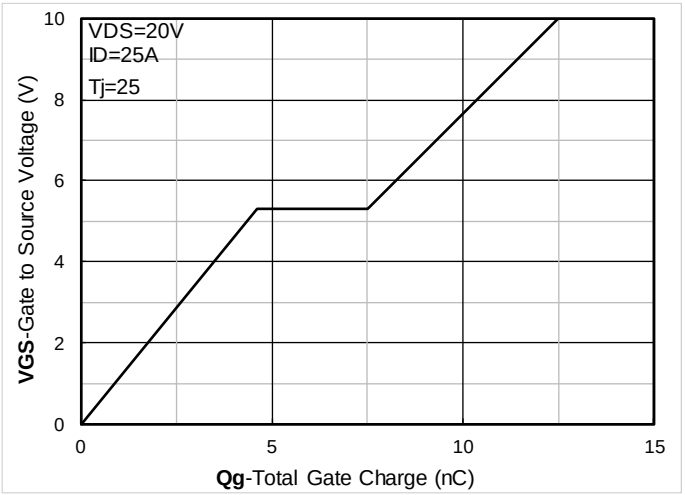



Figure 4. Gate Charge

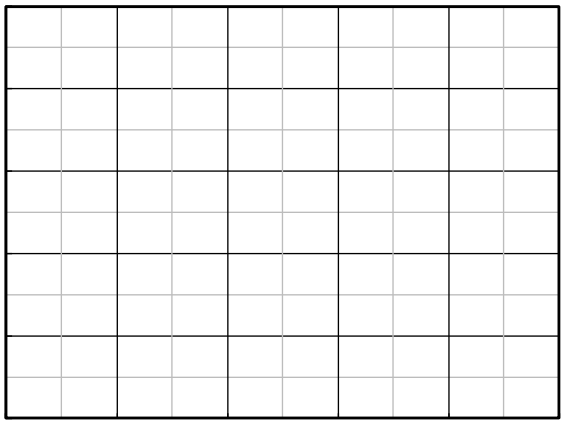


Figure 5. On-Resistance vs Gate to Source Voltage

Figure 6. Normalized On-Resistance

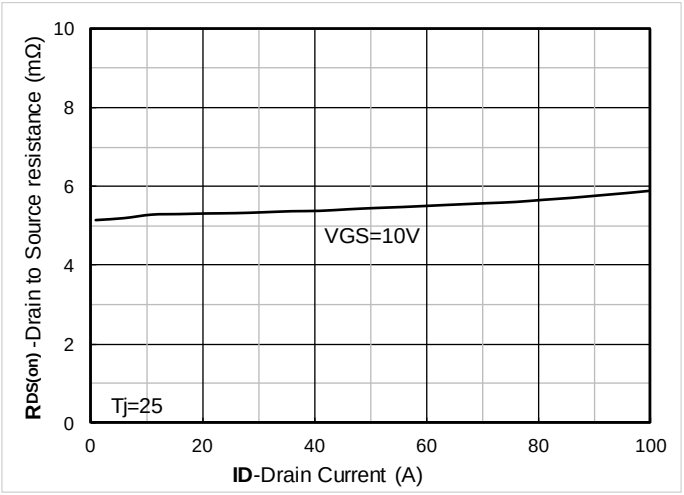



Figure 7. $R_{DS(on)}$ VS Drain Current

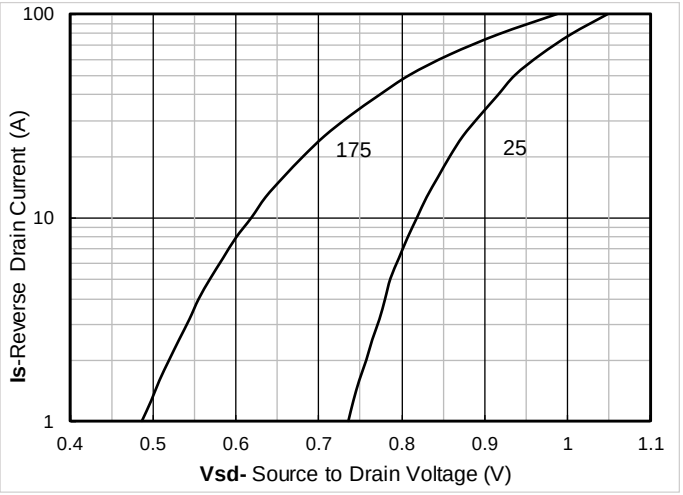



Figure 8. Forward characteristics of reverse diode

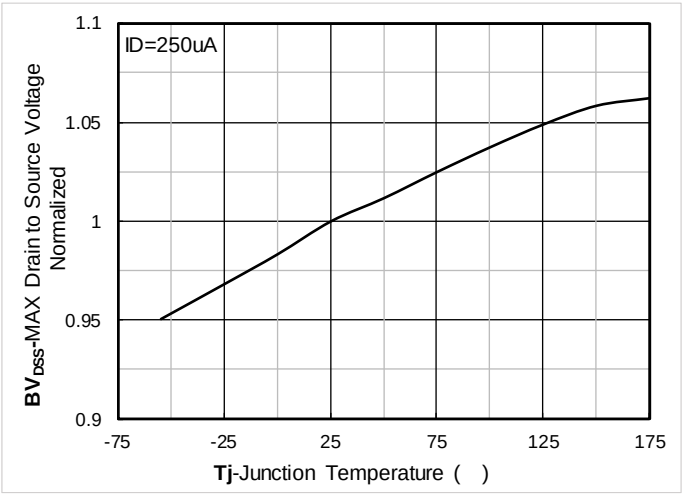



Figure 9. Normalized breakdown voltage

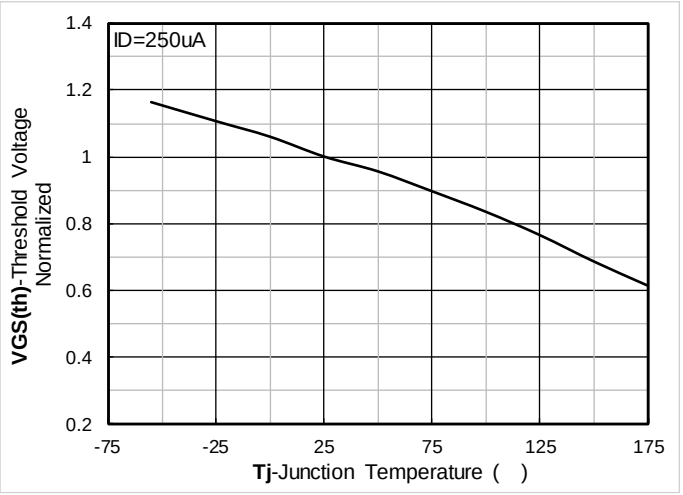



Figure 10. Normalized Threshold voltage

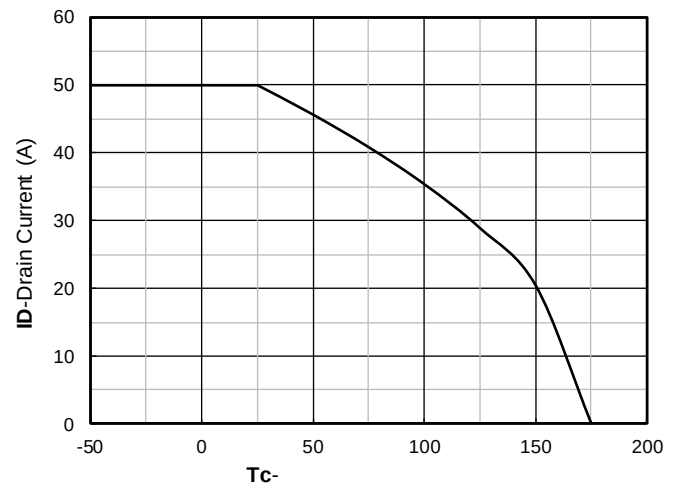



Figure 11. Current dissipation

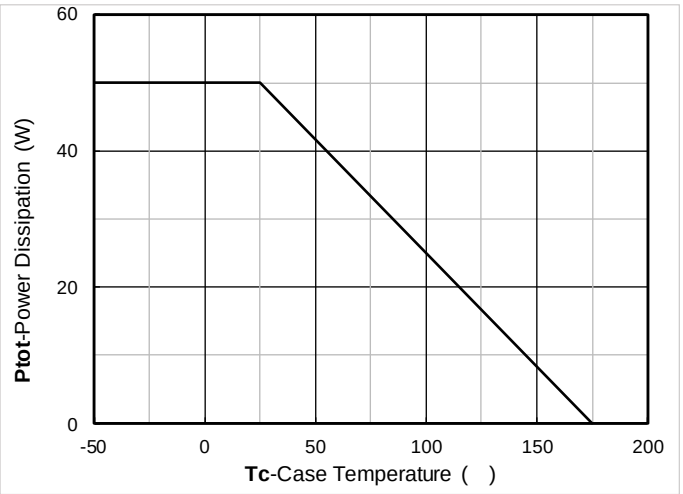
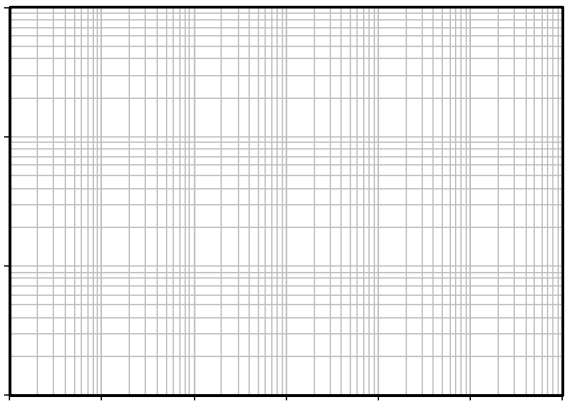



Figure 12. Power dissipation



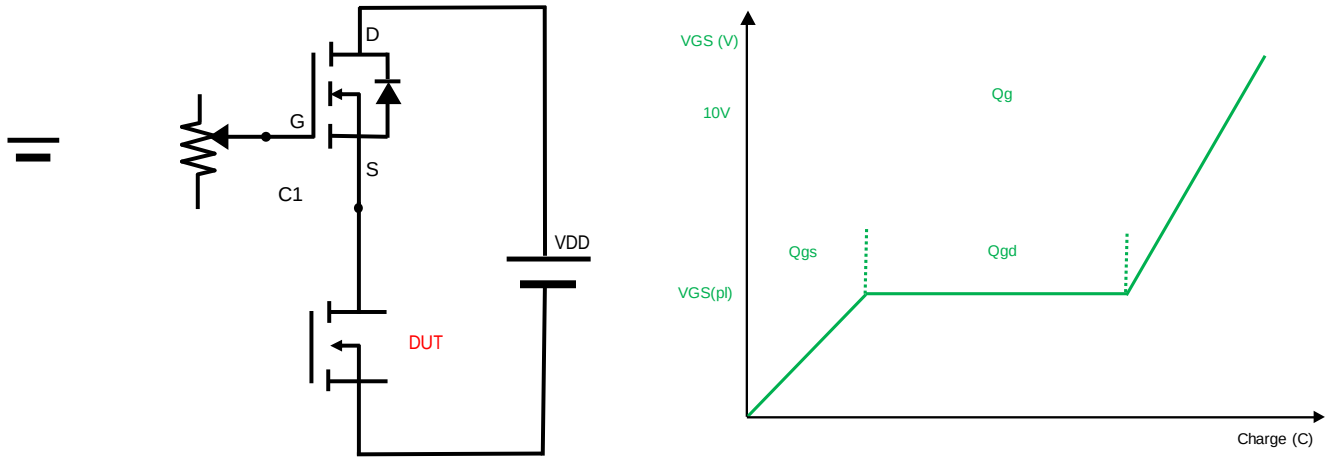



Figure B. Gate Charge Test Circuit & Waveform

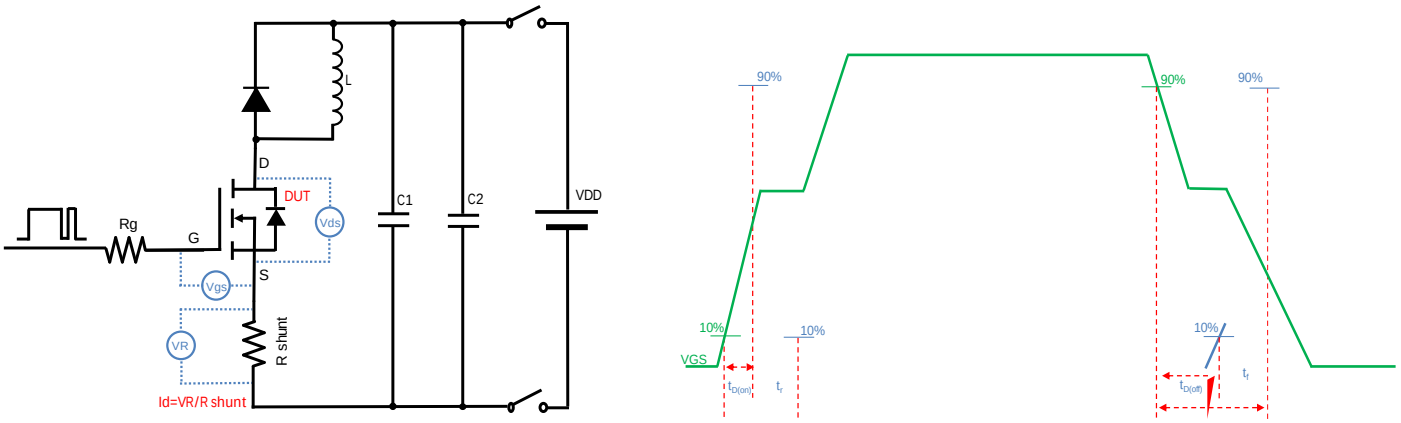



Figure C. Resistive Switching Test Circuit & Waveform

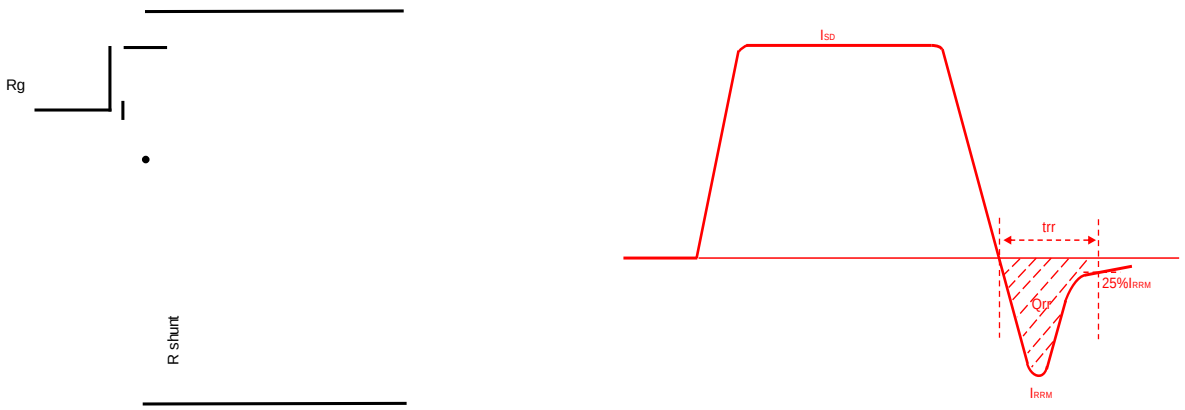
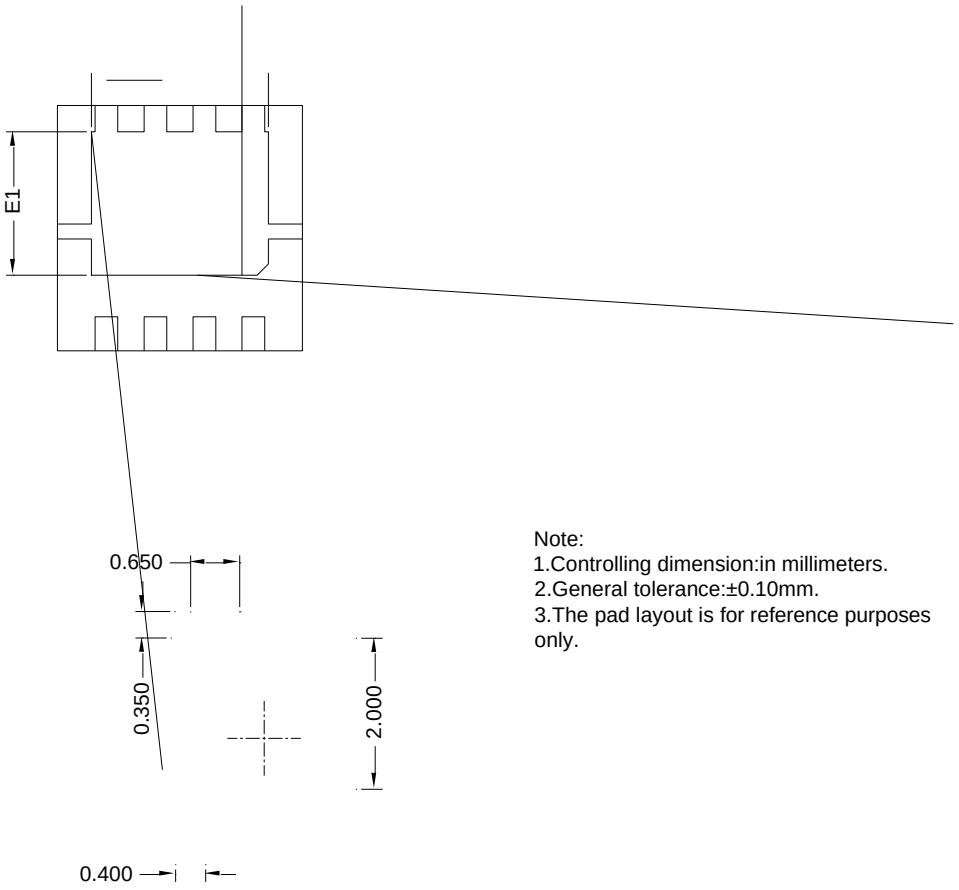



Figure D. Diode Recovery Test Circuit & Waveform

## ■ DFN3333-8L-A-0.8MM Package information




Suggested Solder Pad Layout
Top View

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

**Disclaimer**