P-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	-100V
I_D	-16A
$R_{DS(ON)}$(at V_{GS}=-10V)	85m
$R_{DS(ON)}$(at V_{GS}=-4.5V)	102m

100% EAS Tested

100% V_{DS} Tested

General Description

Trench Power MOSFET technology

Excellent package for heat dissipation

High density cell design for low $R_{DS(ON)}$

”Moisture Sensitivity Level 1

Epoxy Meets UL 94 V-0 Flam EMC /P /AMCID 61/Langk5.67rrelsivR4(

■Typical Electrical and Thermal Characteristics Diagrams

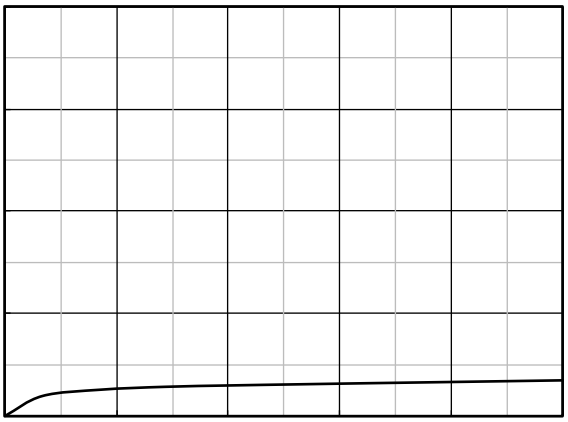


Figure 1. Output Characteristics

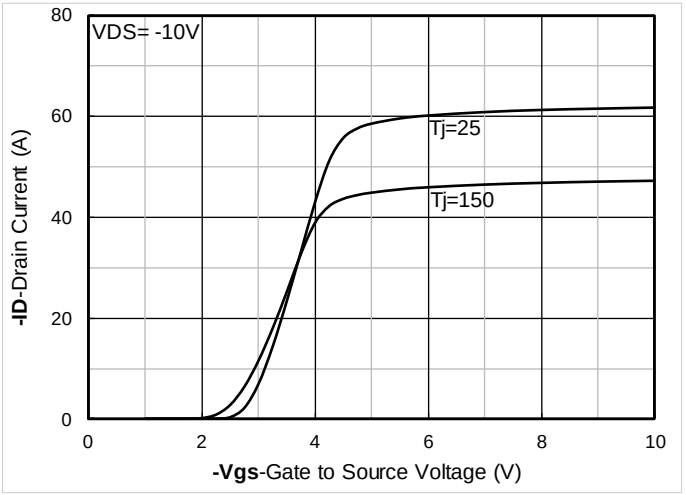


Figure 2. Transfer Characteristics

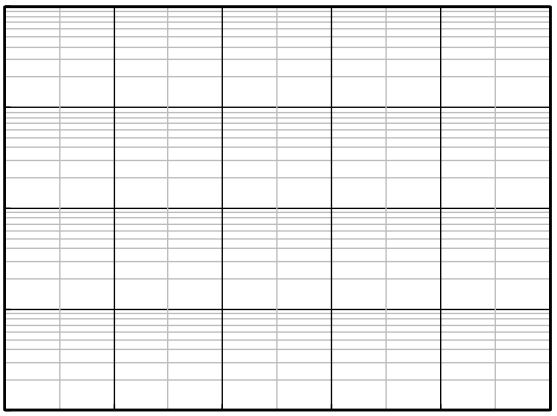
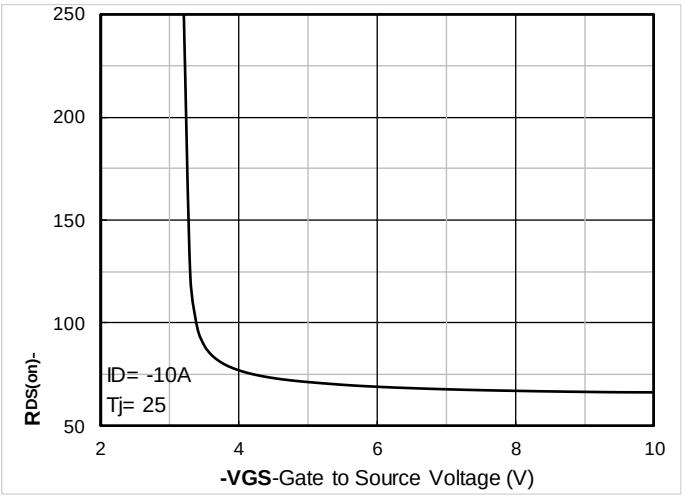


Figure 3. Capacitance Characteristics

Figure 4. Gate Charge



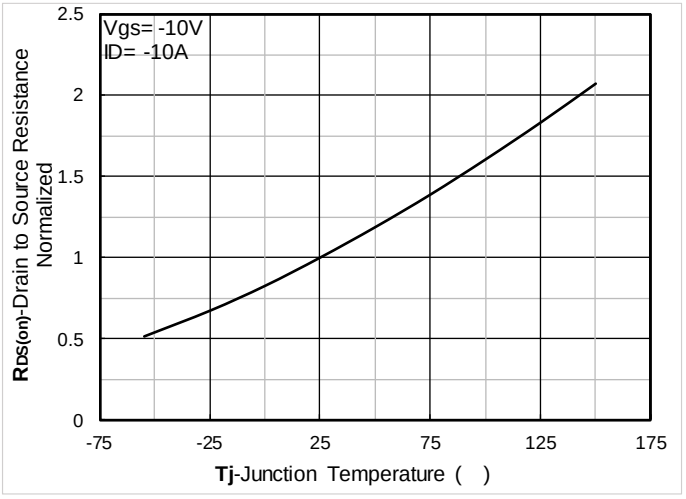


Figure 5.

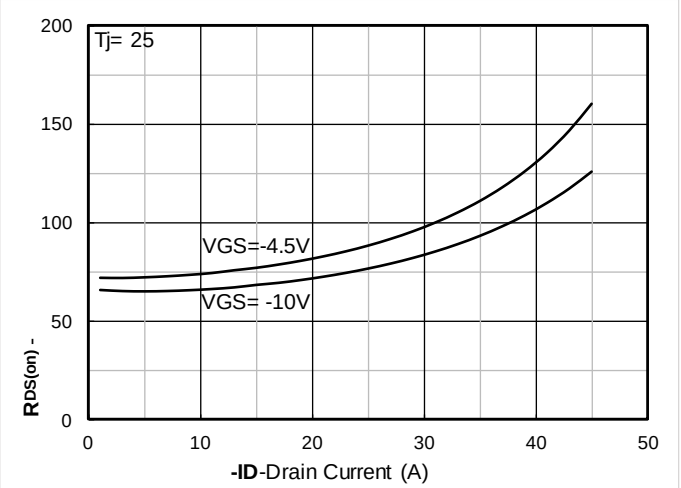


Figure 7. $R_{DS(on)}$ VS Drain Current

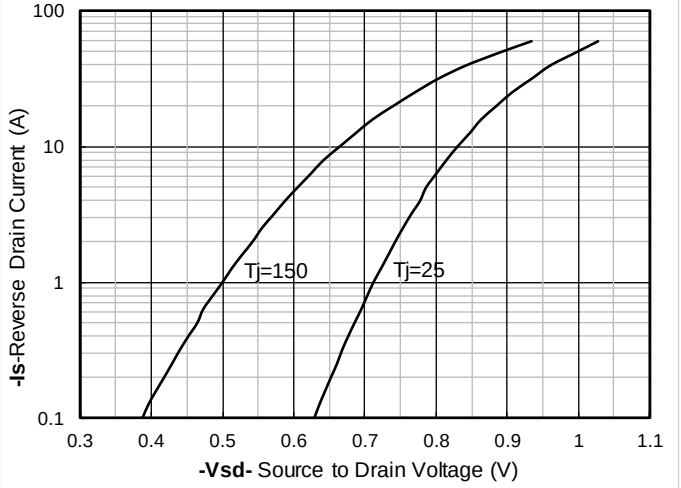


Figure 8. Forward characteristics of reverse diode

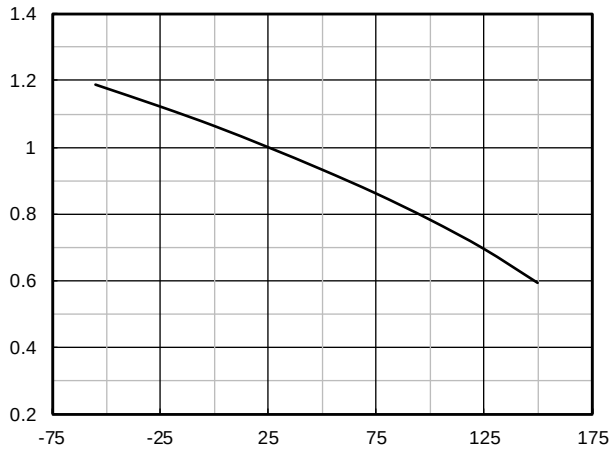


Figure 9. Normalized breakdown voltage

Figure 10. Normalized Threshold voltage

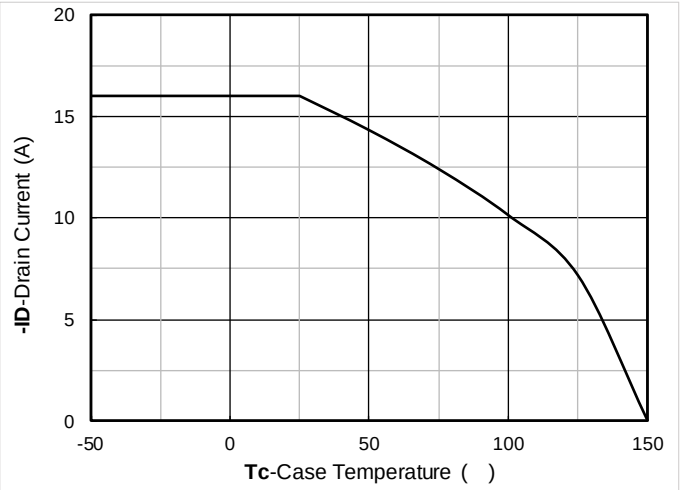


Figure 11. Current dissipation

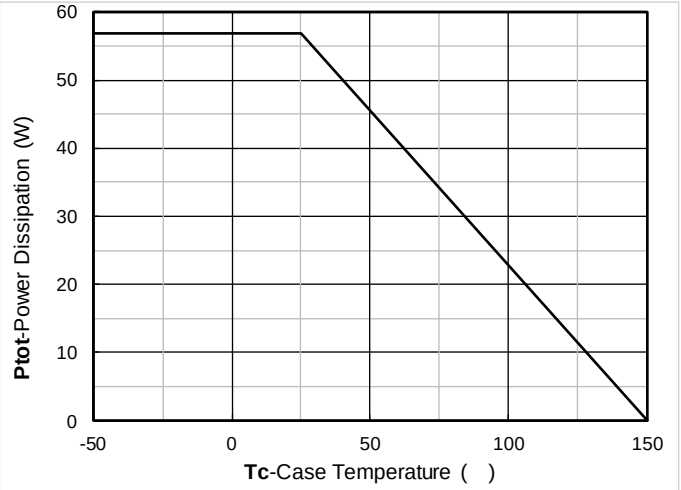


Figure 12. Power dissipation

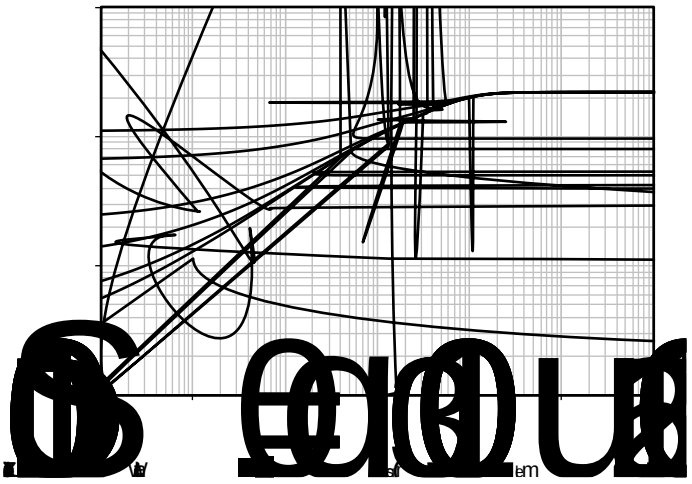


Figure 13. Maximum Transient Thermal Impedance

Figure 14. Safe Operation Area

DFN3333-8L-WF Package information