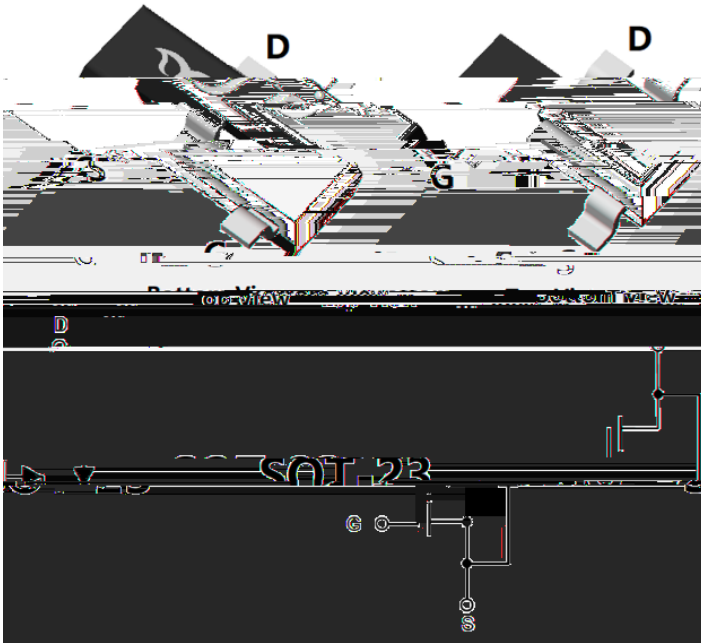




P-Channel Enhancement Mode Field Effect Transistor



Product Summary

V_{DS}	-30V
I_D	-4.1A
$R_{DS(ON)}$ (at $V_{GS}=-10V$)	49mohm
$R_{DS(ON)}$ (at $V_{GS}=-4.5V$)	65mohm

General Description

Trench Power LV MOSFET technology
High density cell design for Low $R_{DS(ON)}$
High Speed switching
Part no. with suffix "Q" means AEC-Q101 qualified

Applications

Battery protection
Load switch
Power management

Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-source Voltage	V_{DS}	-30	V	
Gate-source Voltage	V_{GS}	± 20	V	
Drain Current	I_D	$T_A=25$	-4.1	A
		$T_A=70$	-3.2	
Pulsed Drain Current ^A	I_{DM}	-15	A	
Total Power Dissipation	P_D	$T_A=25$	1.2	W
		$T_A=70$	0.8	W
Thermal Resistance Junction-to-Ambient ^B	R_{JA}	105	/ W	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 +150		

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJL3407AQ	F2	3407.	3000	30000	120000	7" reel



Typical Performance Characteristics

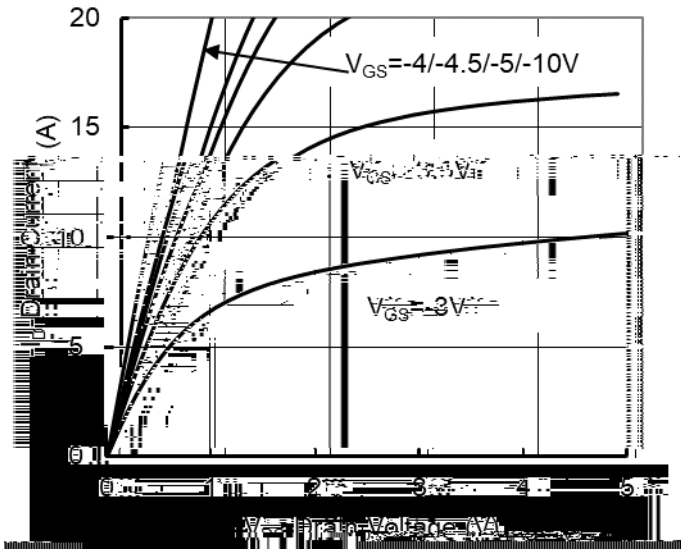


Figure1. Output Characteristics

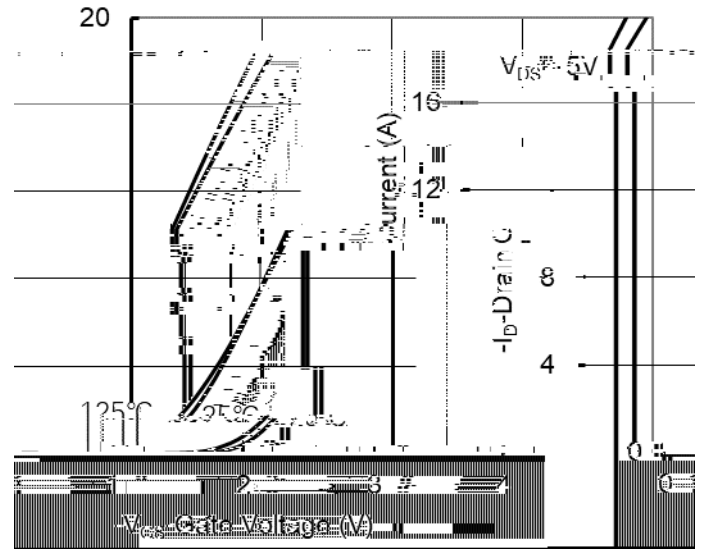


Figure2. Transfer Characteristics

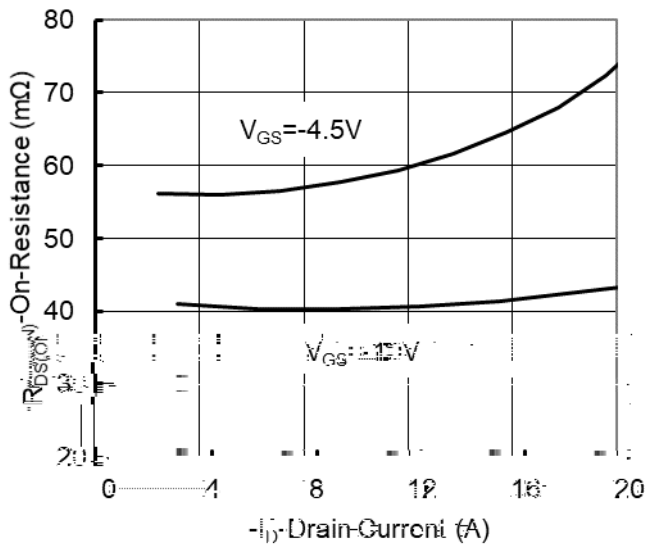


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

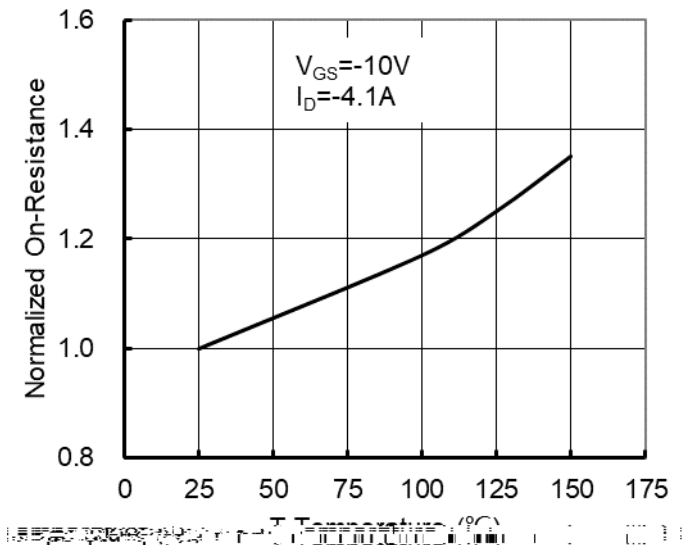


Figure 4: On-Resistance vs. Junction Temperature

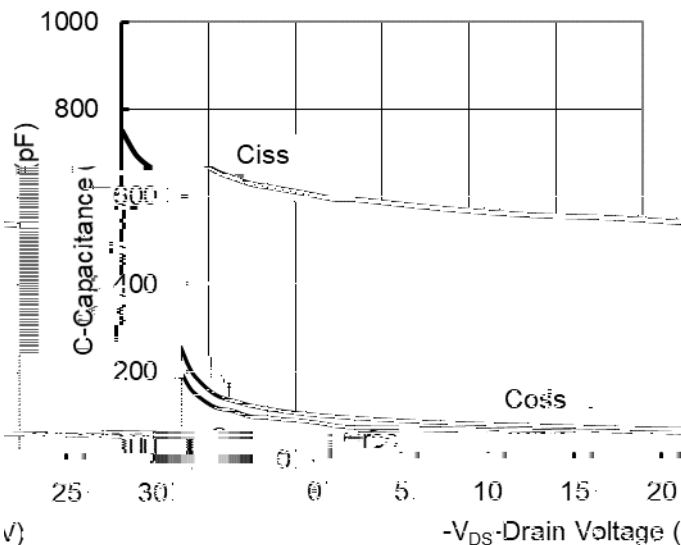


Figure5. Capacitance Characteristics

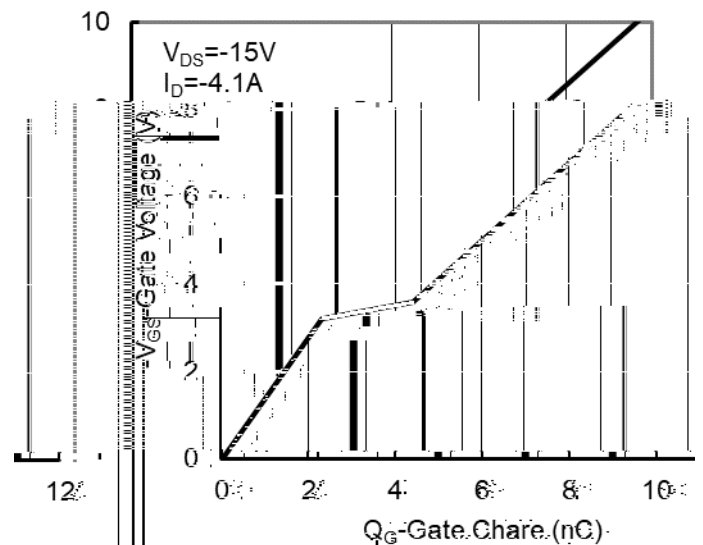


Figure6. Gate Charge

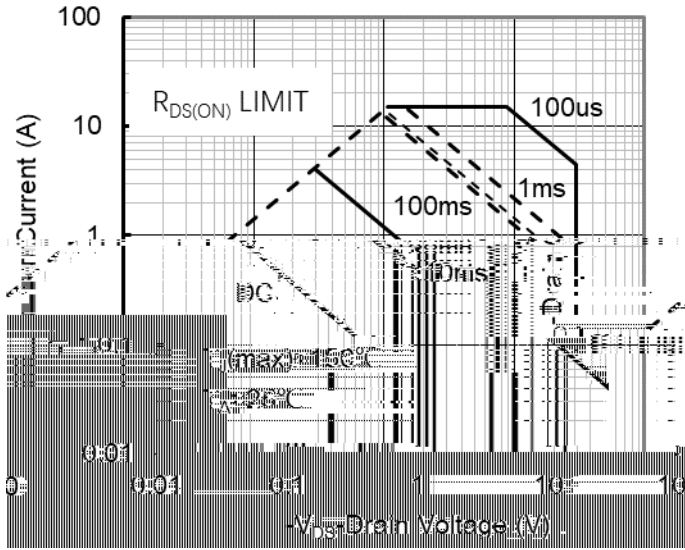


Figure7. Safe Operation Area

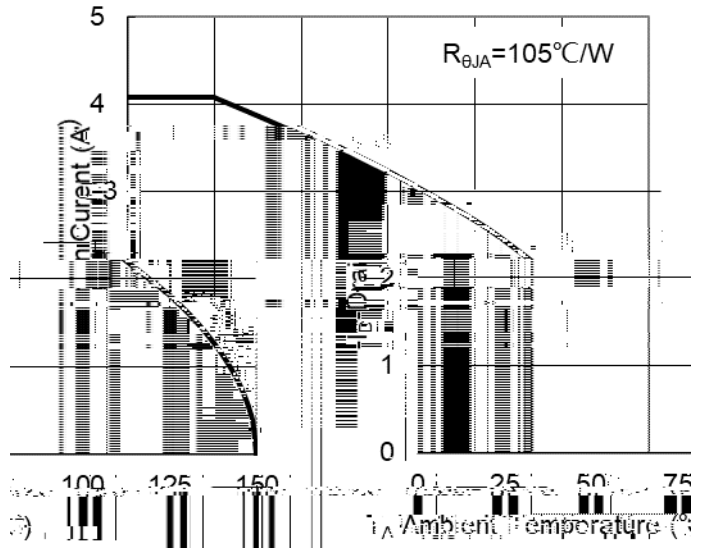


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

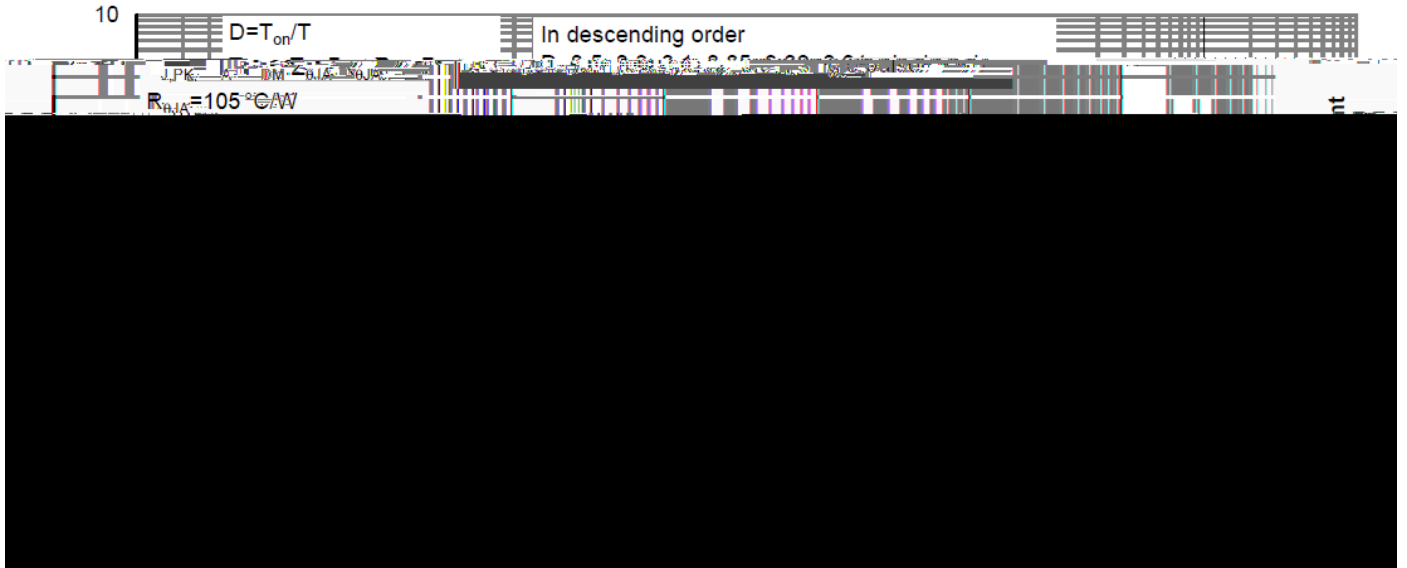
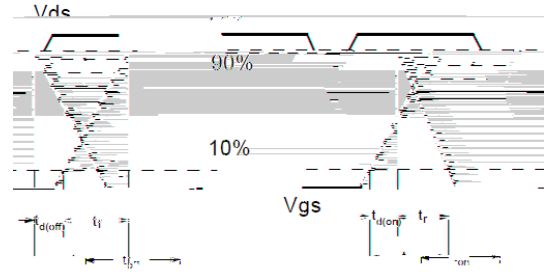
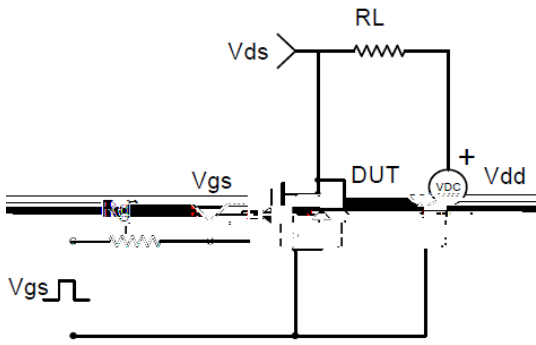
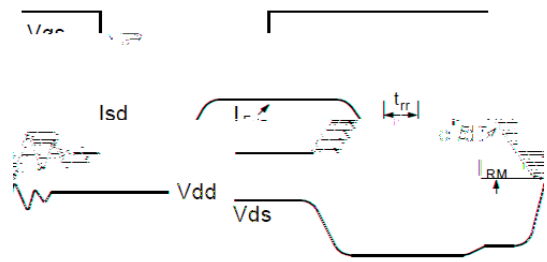
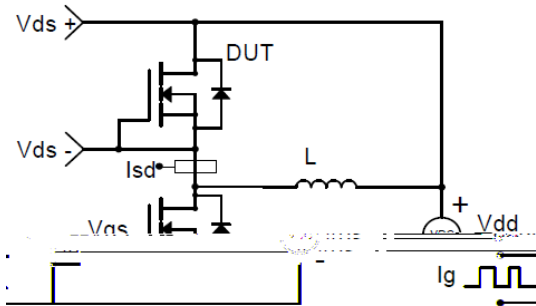


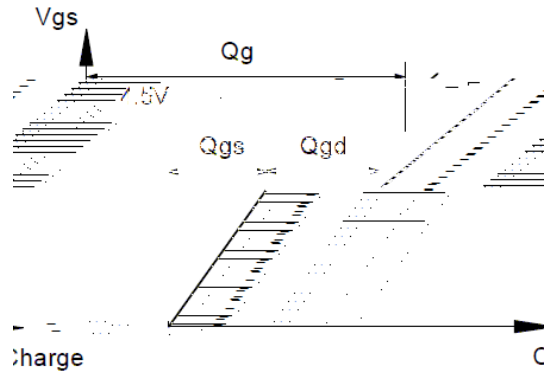
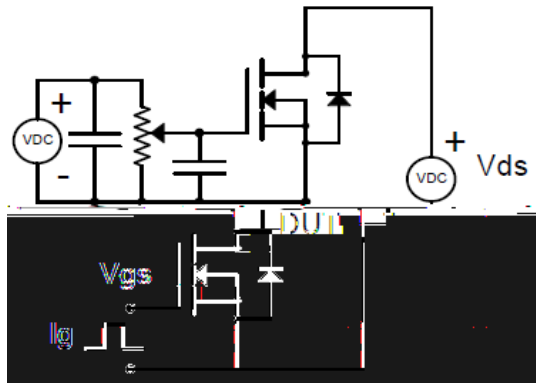
Figure9. Normalized Maximum Transient Thermal Impedance



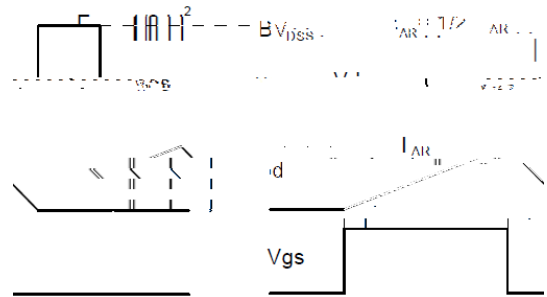
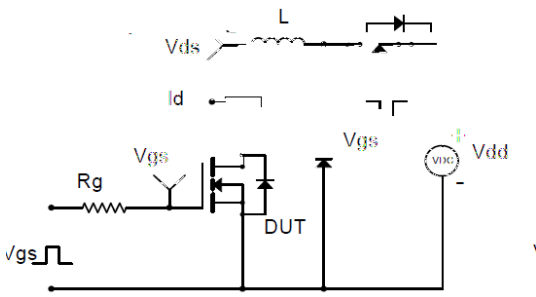
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



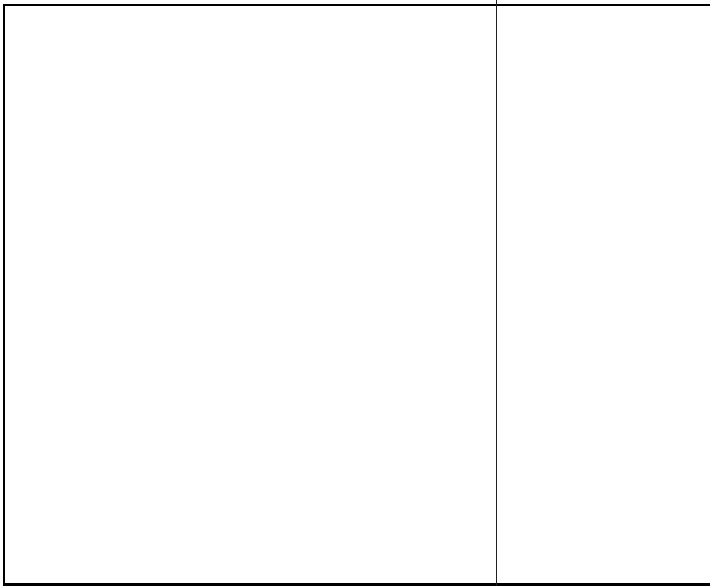
Gate Charge Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

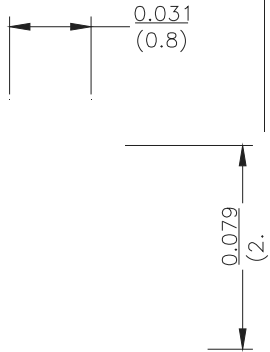
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