



YJGD20N06AQ

NMOS(Die1/Die2) Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1	1.5	2.5	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =20A		23	30	m
		V _{GS} =4.5V, I _D =10A		28	40	m
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V			1.2	V
Gate resistance	R _G	f=1MHz		2		
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1MHz		1250		pF
Output Capacitance	C _{oss}			80		
Reverse Transfer Capacitance	C _{rss}			60		
Switching Parameters						
Gate-Source Charge	Q _{gs}	V _{GS} =10V, V _{DS} =30V, I _D =20A	-	3	-	nC
Gate-Drain Charge	Q _{gd}		-	6	-	
Reverse Recovery Charge	Q _{rr}	I _F =20A, di/dt=100A/us	-	17.5	-	nC
Reverse Recovery Time	t _{rr}		-	23.5	-	ns

Turn-on Delay Time

t_{D(on)}

10
8

V_{GS}=10V, V_{DD}=30V, I_D=20A
Ry f



NMOS(Die1/Die2) Typical Electrical and Thermal Characteristics Diagrams

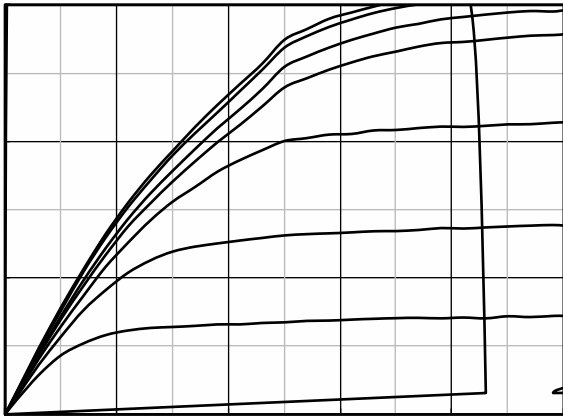


Figure 1. Output Characteristics

Figure 2. Transfer Characteristics

Figure 3. Capacitance Characteristics

Figure 4. Gate Charge

Figure 5. On-Resistance vs Gate to Source Voltage

Figure 6. Normalized On-Resistance



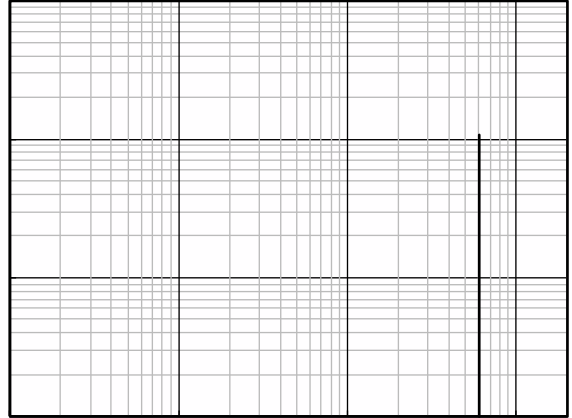


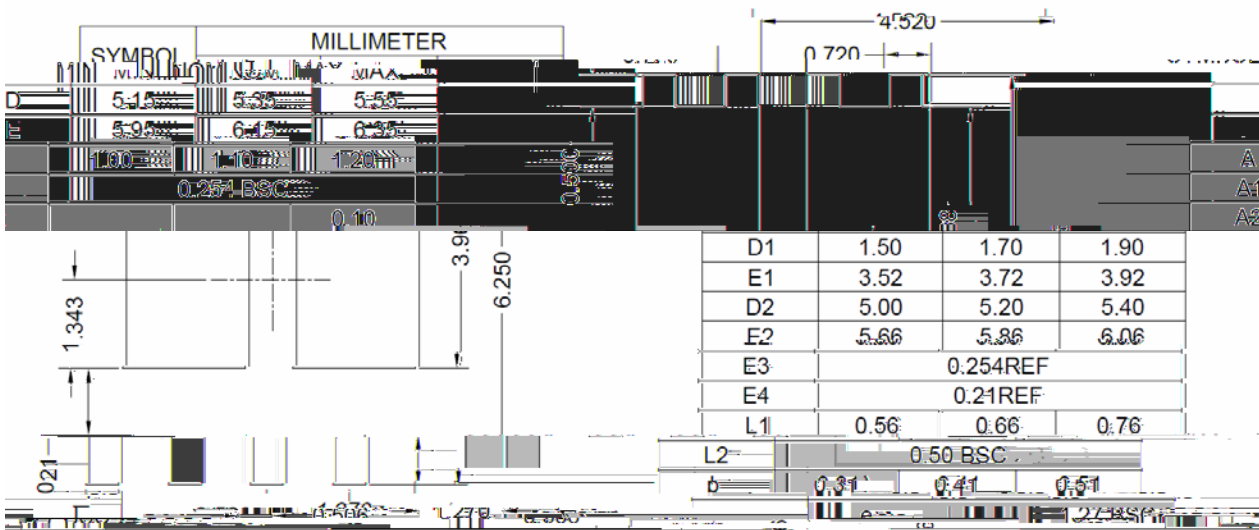
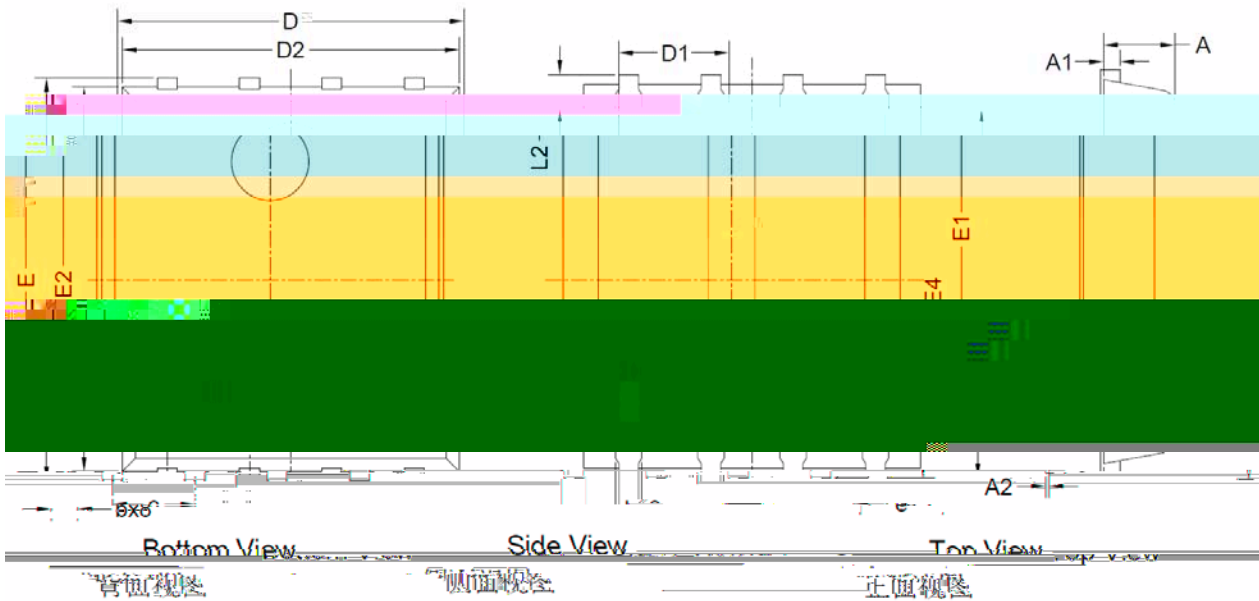
Figure 13. Maximum Transient Thermal Impedance

Figure 14. Safe Operation Area



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PDFN5060-8L-E-1.1MM Package information



1. All dimensions in millimeters.
 2. General tolerance: ± 0.10 mm.
 3. The pad layout is for reference purposes only.

Note:
 Suggested Solder Pad Layout
 Suggested Solder Pad Layout
 1.40



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