N-Channel and N-Channel Complementary MOSFET

Product Summary

- V_{DS} 100V
- I_D 20A
- $R_{DS(ON)}$(at V_{GS}=10V) 19mΩ
- $R_{DS(ON)}$(at V_{GS}=4.5V) 23mΩ
- 100% EAS Tested
- 100% V_{DS} Tested

General Description

- Split gate trench MOSFET technology
- High density cell design for low $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- DC-DC Converters
- Power management functions
- Industrial and Motor Drive application

■ **Absolute Maximum Ratings** (T_A=25

■ Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V	-	-	1	μA
		V_{DS}=100V, V_{GS}=0V, Tj=150	-	-	100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.0	1.8	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	15	19	mΩ
		V_{GS}=4.5V, I_D=7A	-	18	23	
Diode Forward Voltage	V_{SD}	I_S=20A, V_{GS}=0V	-	-	1.2	V
Gate resistance	R_G	f=1MHz	-	1.5	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	20	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=50V, V_{GS}=0V, f=1MHz	-	1150	-	pF
Output Capacitance	C_{oss}		-	430	-	
Reverse Transfer Capacitance	C_{rss}		-	8	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V, V_{DS}=50V, I_D=20A	-	20	-	nC
Gate-Source Charge	Q_{gs}		-	5.6	-	
Gate-Drain Charge	Q_{gd}		-	2.8	-	
Reverse Recovery Charge	Q_{rr}	I_F=20A, di/dt=100A/us	-	32	-	nC
Reverse Recovery Time	t_{rr}		-	41	-	ns

Typical Electrical and Thermal Characteristics Diagrams

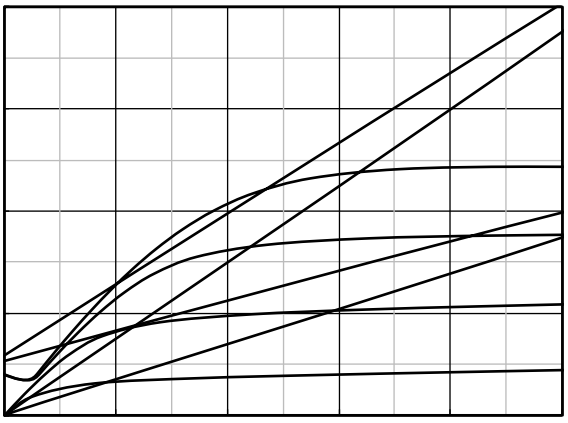
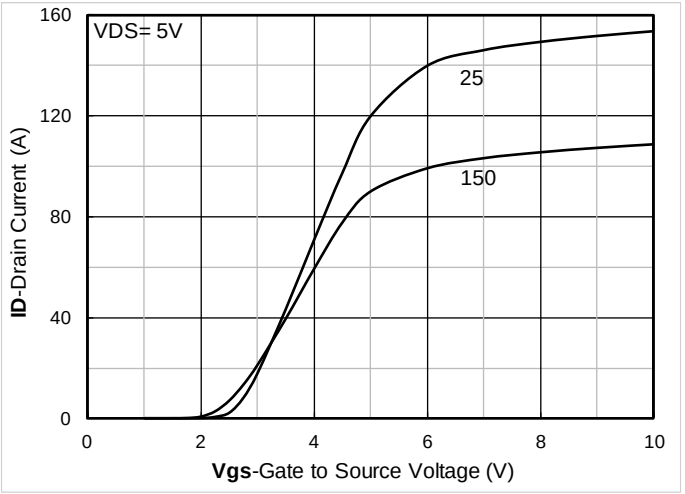


Figure 1. Output Characteristics



Figure

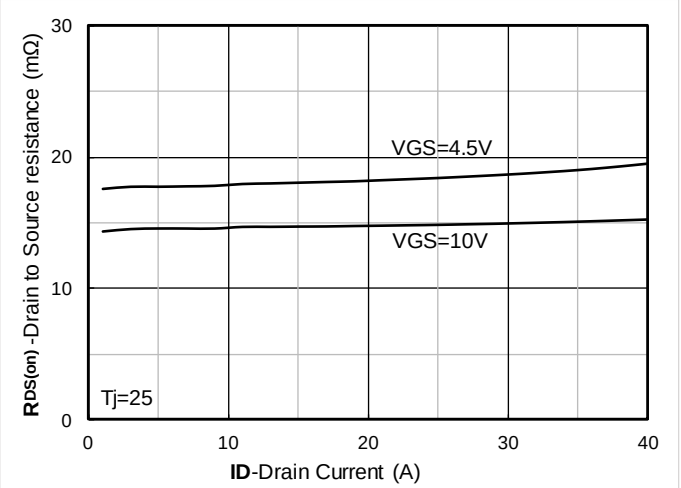


Figure 7. $R_{DS(on)}$ VS Drain Current

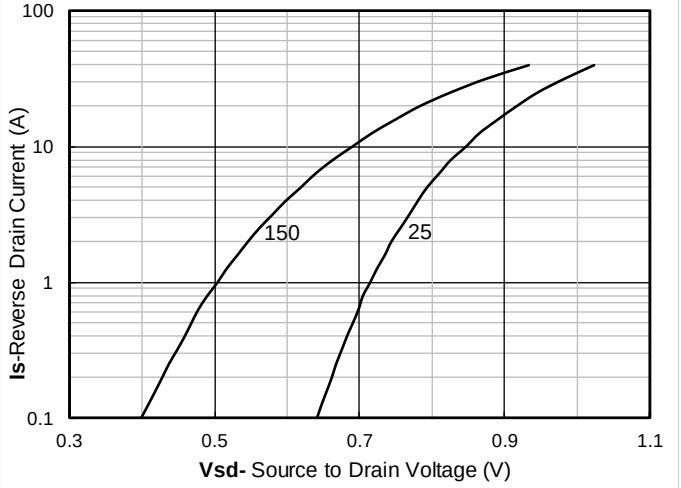


Figure 8. Forward characteristics of reverse diode

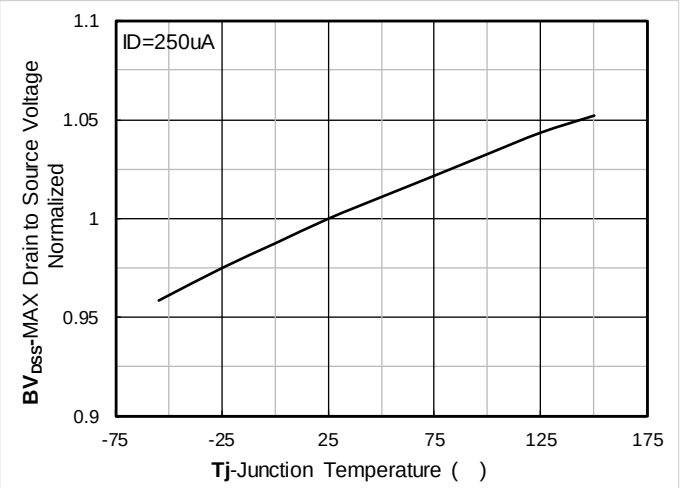


Figure 9. Normalized breakdown voltage

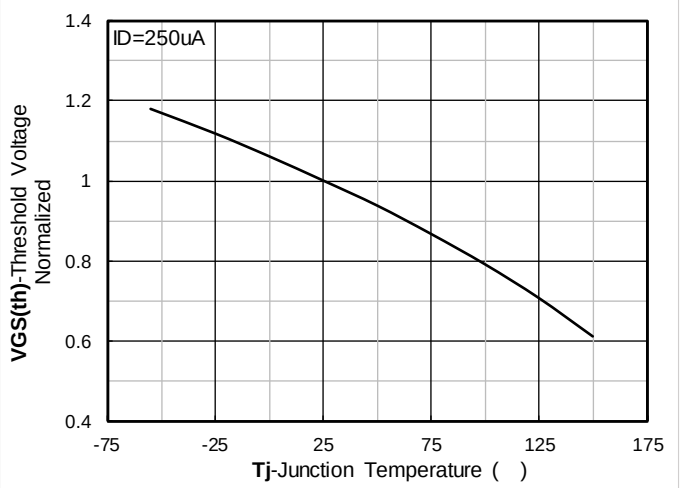


Figure 10. Normalized Threshold voltage

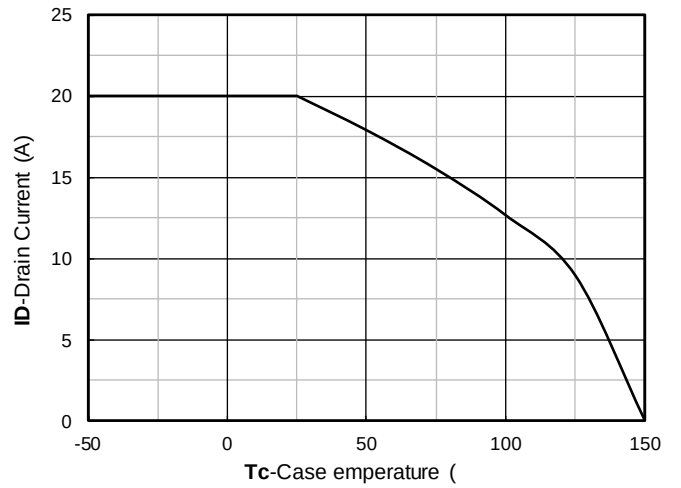


Figure 11. Current dissipation

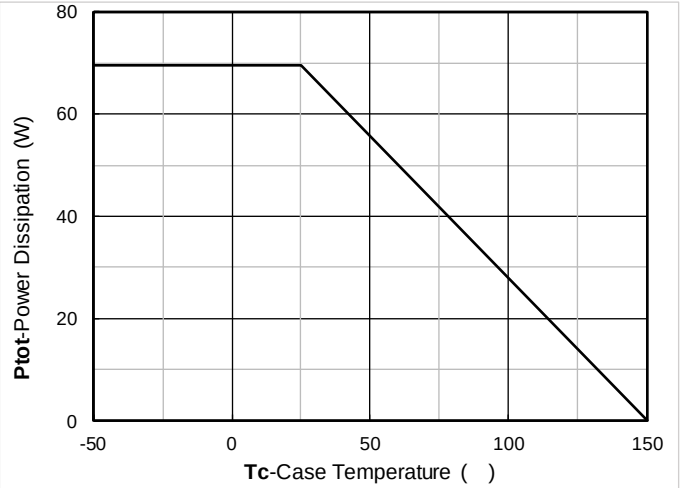


Figure 12. Power dissipation

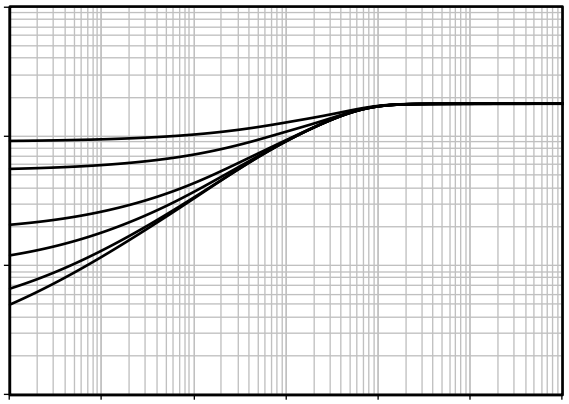


Figure 13. Maximum Transient Thermal Impedance

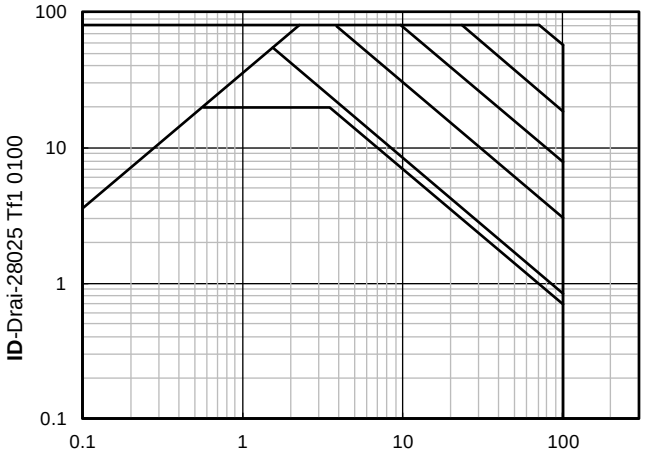


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

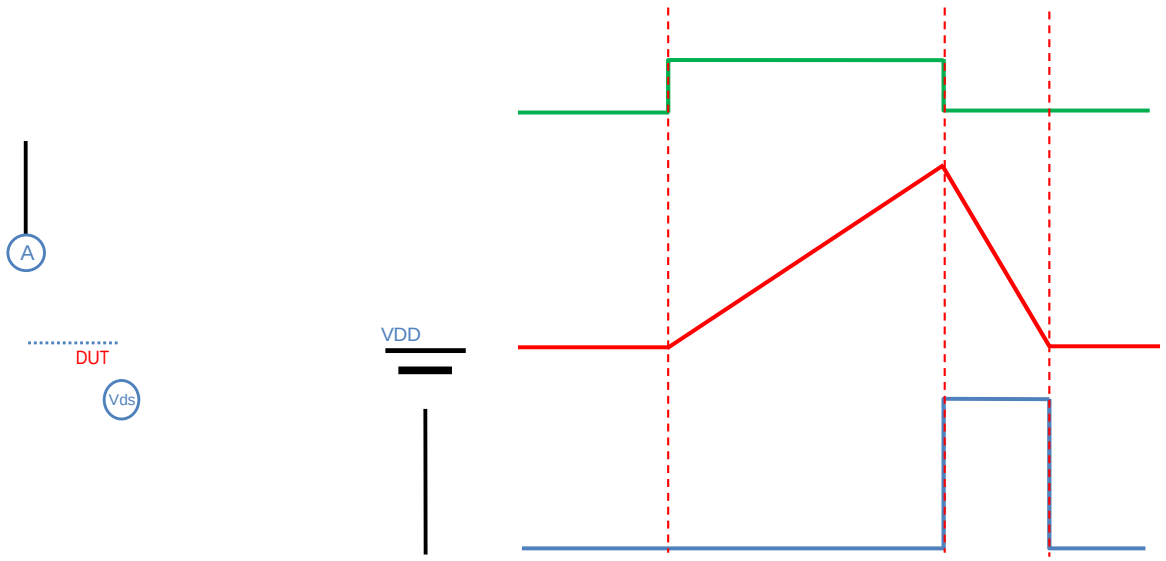


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

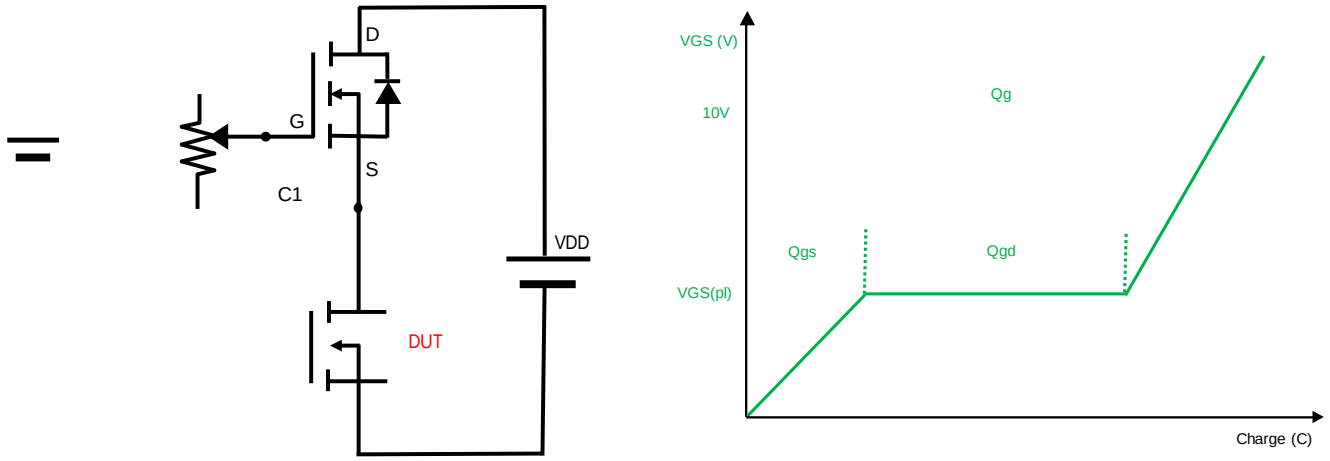


Figure B. Gate Charge Test Circuit & Waveform

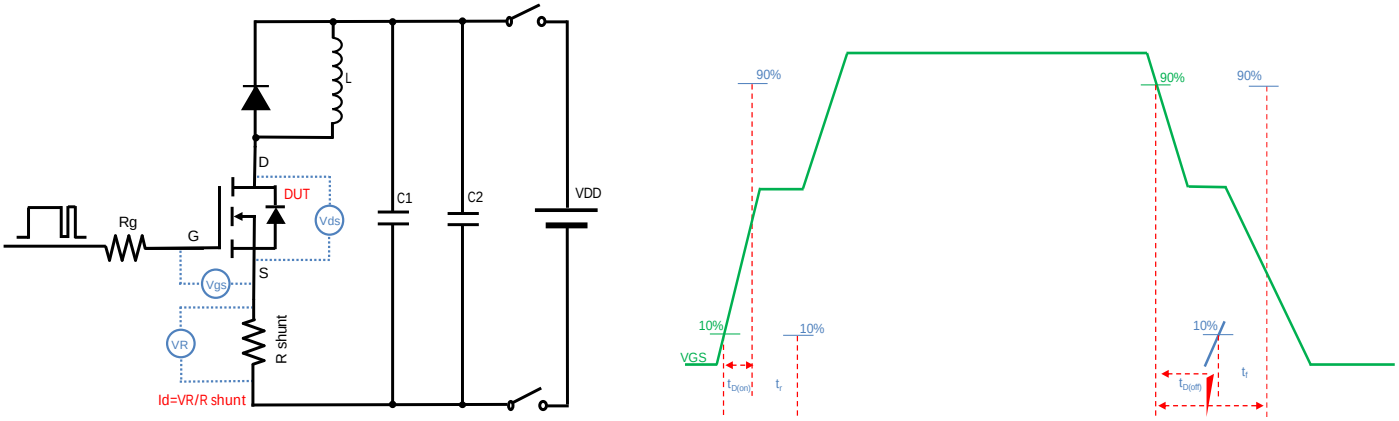


Figure C. Resistive Switching Test Circuit & Waveform

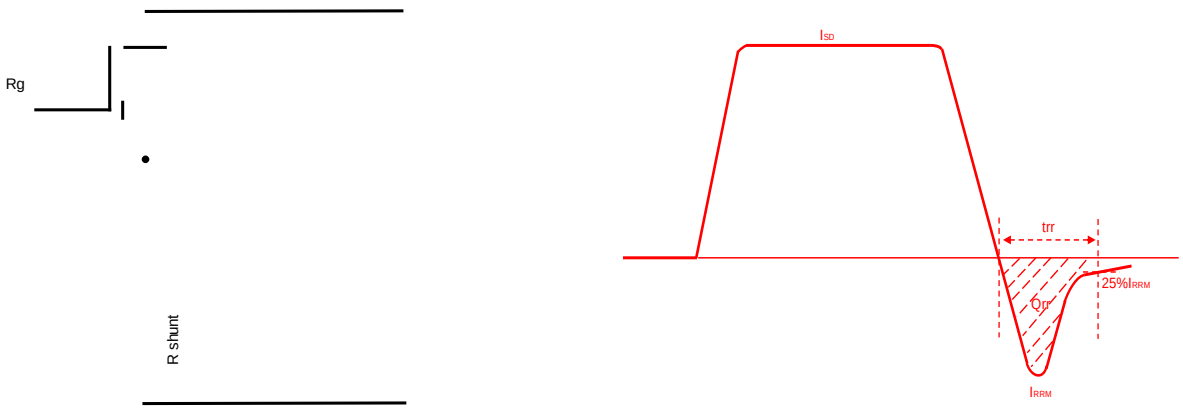
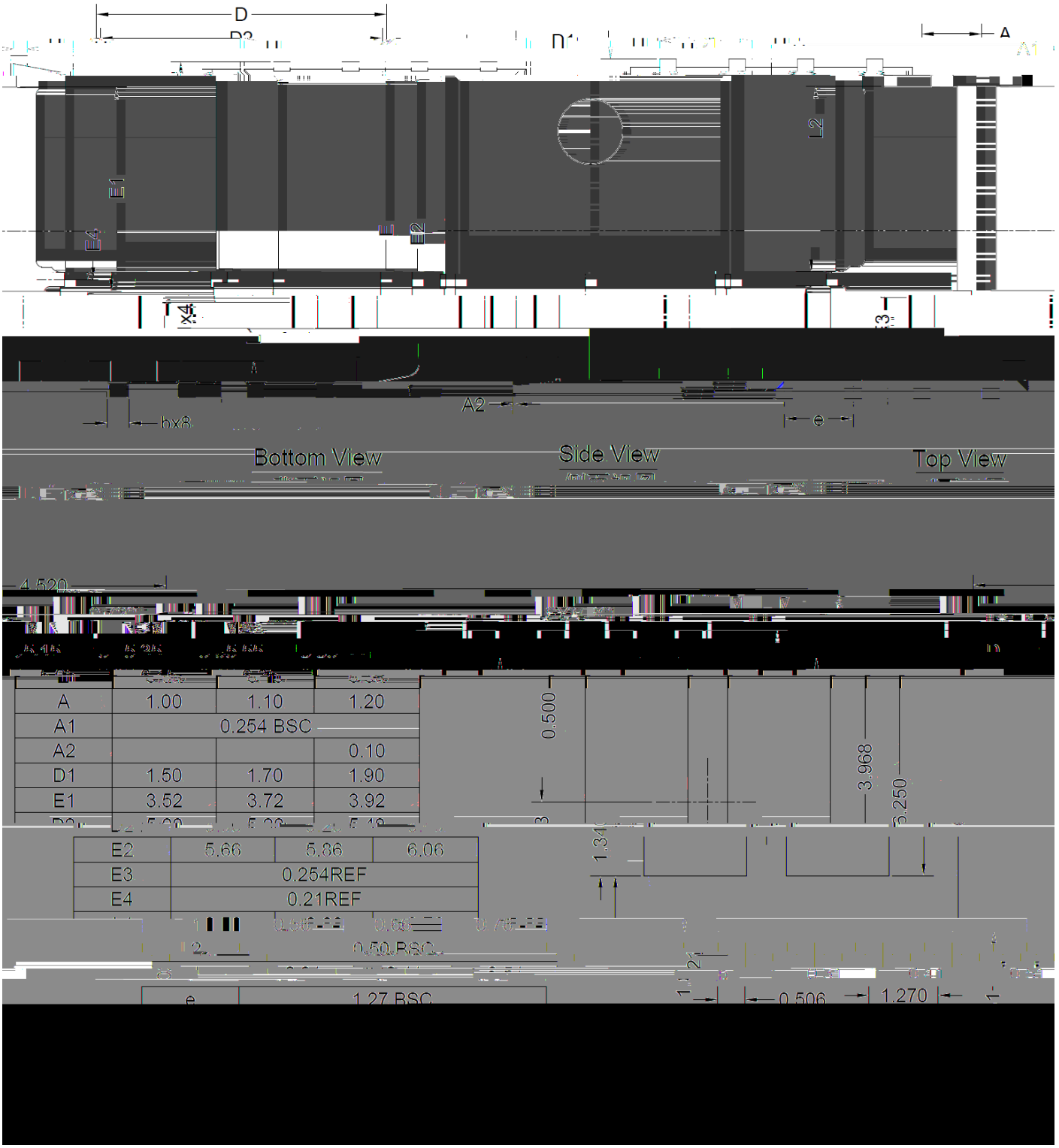


Figure D. Diode Recovery Test Circuit & Waveform

■ PDFN5060-8L-E-1.1mm Package information



A	1.00	1.10	1.20
A1		0.254 BSC	
A2			0.10
D1	1.50	1.70	1.90
E1	3.52	3.72	3.92
E2	5.66	5.86	6.06
E3		0.254REF	
E4		0.21REF	

Disclaimer

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