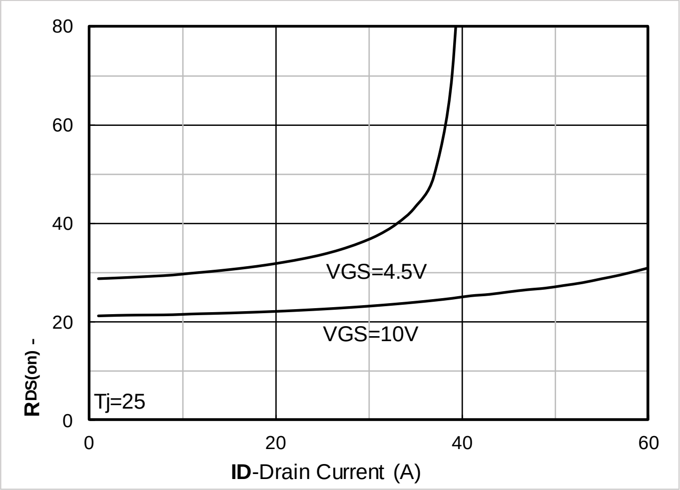
N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	100V
I_D	27A
$R_{DS(ON)}$(at V_{GS}=10V)	29m
$R_{DS(ON)}$(at V_{GS}=4.5V)	47m
100% EAS Tested	
100% V_{DS} Tested	

YJD27G10A



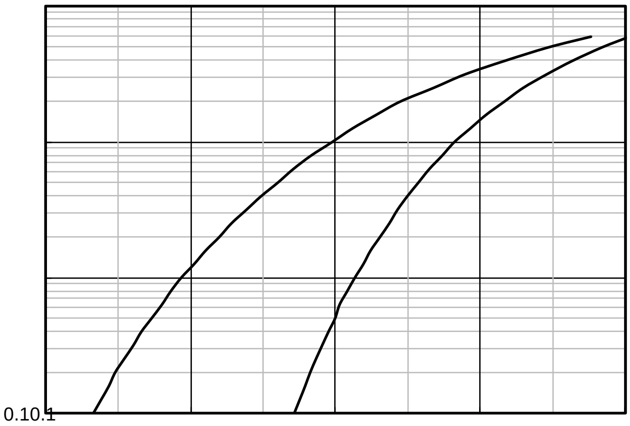
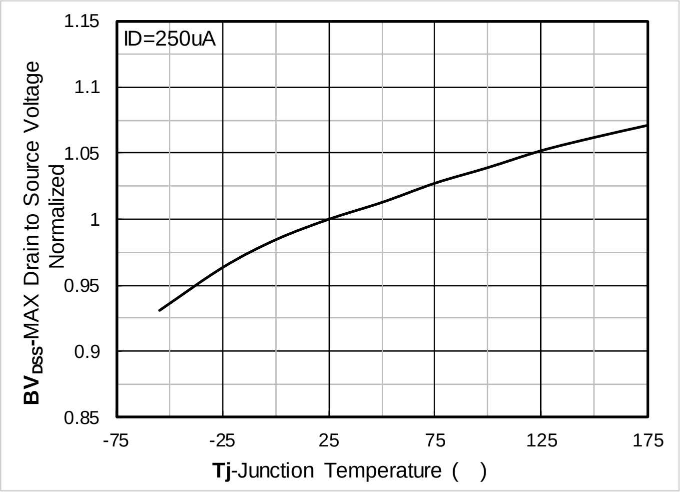


Figure 7. RDS(on) VS Drain Current

Figure 8. Forward characteristics of reverse diode



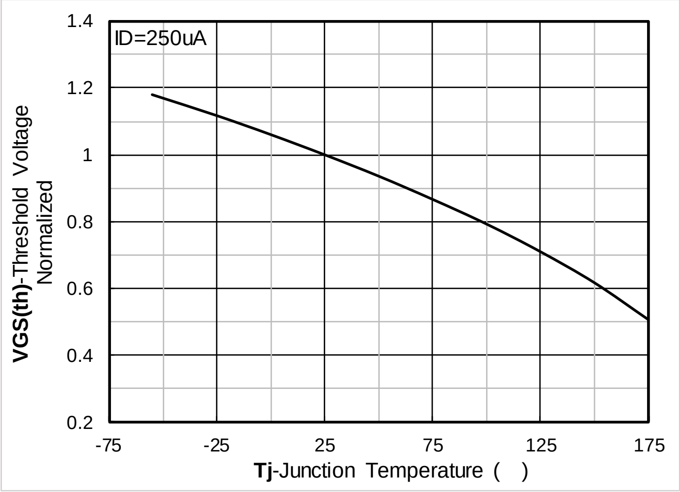


Figure 9. Normalized breakdown voltage

t -120【)-70 0 G【)]TJETQq0.000008882 0 596.04 842.04 reW* nBT

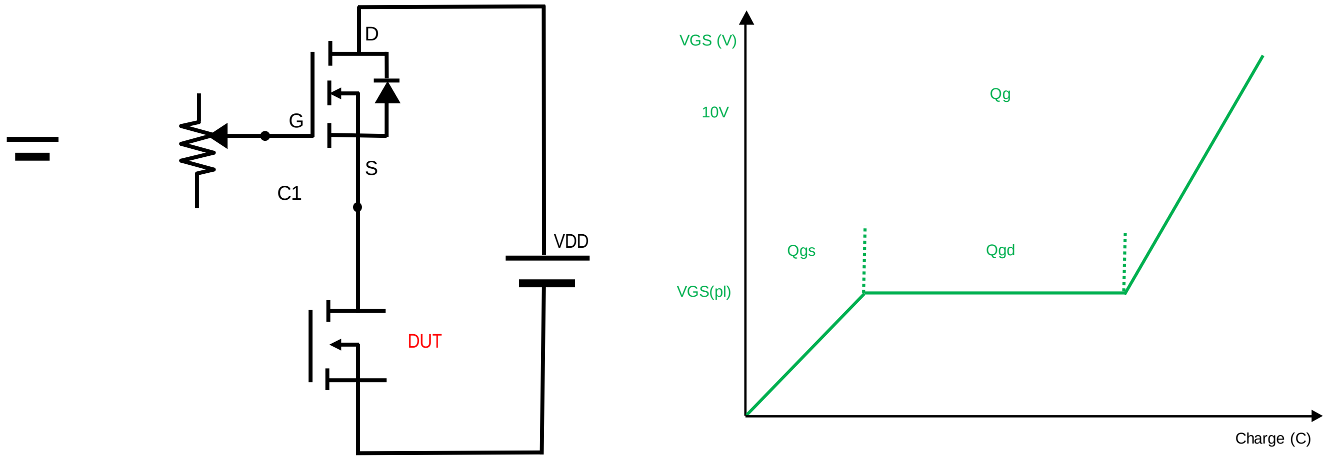


Figure B. Gate Charge Test Circuit & Waveform

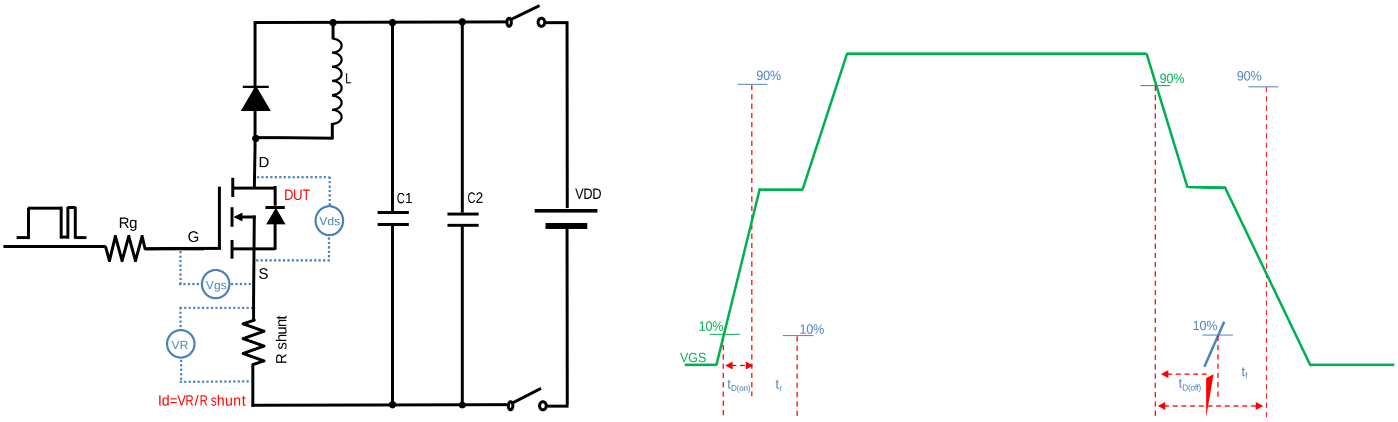


Figure C. Resistive Switching Test Circuit & Waveform

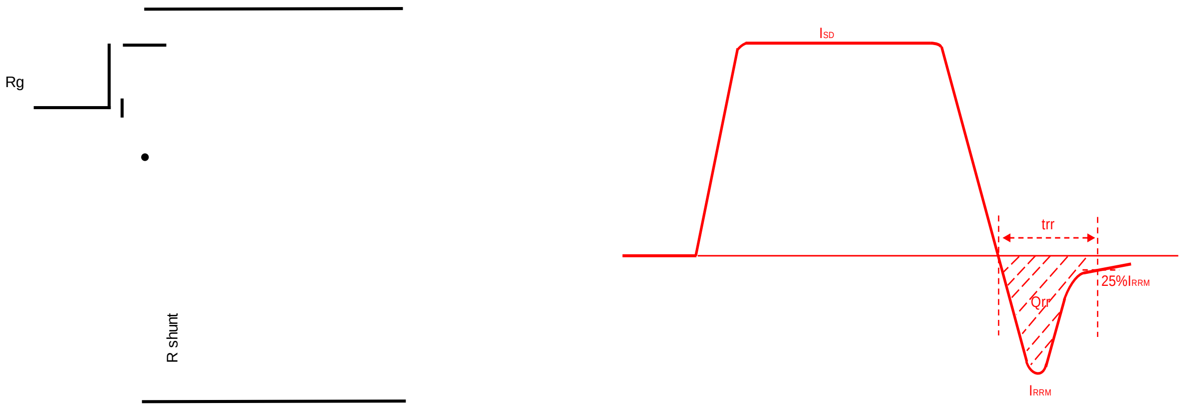
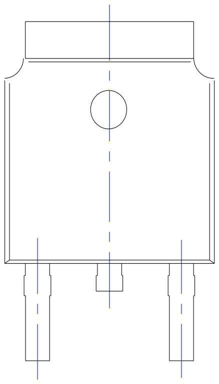
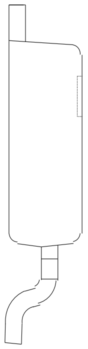


Figure D. Diode Recovery Test Circuit & Waveform

TO-252-B Package information

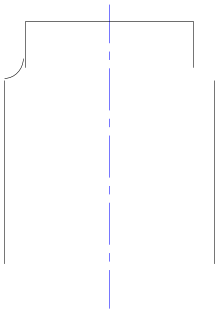


TOP VIEW



SIDE VIEW

	DIMENSIONS				
SYMBOL	INCHES				
	MIN.	NOM.			
A1	0.000				
A2	0.087	0.091			
A3	0.035	0.039			
b	0.026	0.030			
c	0.018	0.020			
D	0.256	0.260			
D1					
D2	0.181	0.189			
E	0.390	0.398			
E1	0.236	0.240			



BOTTOM VIEW

SUGGESTED SOLDER PAD LAYOUT

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.